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Full Length Article

Performance analysis of FPGA controlled four-leg DSTATCOM for multifarious load compensation in electric distribution system

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ABSTRACT

A field programmable gate array (FPGA) controlled four-leg distribution static compensator (FL-DSTATCOM) has been implemented to achieve harmonic alleviation, supply current balancing, compensation of reactive power and current flow in the neutral conductor of a 4-wire 3-phase electric distribution system with static, dynamic and combined loads. The unbalanced non-linear and linear static loads are considered for analyzing compensation behaviour of FL-DSTATCOM. The practicability of FL-DSTATCOM for compensating reactive power under dynamic condition is evaluated with slip ring induction machine having variable load current. Also, the performance of FL-DSTATCOM is examined with combined load, which is a combination of dynamic and unbalanced static loads. The reference current signals are produced by using synchronous reference frame theory. Hysteresis band current controller is utilized for generating switching pulse for IGBT switches present in the FL-DSTATCOM. Independent modules are developed for realizing all the tasks in FPGA with the feasibility to reconfigure the hardware for any other application with similar requirements. The experimental results demonstrate that the FPGA controlled FL-DSTATCOM is capable of making the supply current as balanced and sinusoidal, maintaining the power factor at point of common coupling near to unity and reducing the supply neutral current very close to zero.

1. Introduction

During power distribution, the 4-wire 3-phase electric distribution system (EDS) faces several issues on power quality (PQ) such as reactive, harmonic and neutral current flow and impermissible voltage drop owing to unbalanced non-linear/ linear loads [1]. These loads include electric arc furnaces, welding machines, computers, speed drivers in air conditioners, industrial pumps and other microprocessor based equipment, lighting load, house hold applications, laser printer, switched mode power supply, large uninterrupted power supply, boring machines, lathe, fans, refrigerators and so on. Similarly, the non-linear solid state converters are one of the major reason for injecting the harmonics into the EDS, which affects the performance and leads to increased losses, poor efficiency and inadequate utilization of the EDS [2].

Various custom power devices (CPD) are addressed in [3] to enhance the quality of power in 4-wire 3-phase EDS. The power flow in the electric power distribution line could be effectively controlled with the help of ultimate CPD like distribution static compensator (DSTATCOM). The DSTATCOM is very attractive and it has a good cost-effective solution to minimize the PQ impact in EDS [4]. Various types of DSTATCOM topologies have been reported for neutral current compensation (NCC) and alleviating the PQ issues in EDS [5–7]. The split capacitor based three leg DSTATCOM, special transformer based DSTATCOM and four-leg distribution static compensator (FL-DSTATCOM) based topologies are broadly employed for NCC in systems with unbalanced/ balanced non-linear and linear loads. FL-DSTATCOM topology outweighed the others in terms of DC link voltage utilization and harmonic mitigation performance [5,8]. It has simple power circuit compared to other topologies and more control flexibility [9,10]. To ensure the PQ of the EDS, FL-DSTATCOM could be installed in between the supply and loads, at appropriate nodes.

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The digital implementation of control algorithm is essential to obtain a proper functioning of the FL-DSTATCOM. The advanced digital controllers like digital signal processors (DSPs), microprocessors, dSPACE and field-programmable gate arrays (FPGAs) are mostly preferred to implement digital controllers for solid state power converters. The capabilities of analog to digital converter (ADC), high processing power and more than required quantities of digital inputs/ outputs make these advanced control technologies a very attractive and effective selection for solid state power converters based applications.

Nowadays, the DSP and microprocessor are facing more complicating and fundamental challenge. These digital controllers have problems like delay in the calculation of the optimal switching state and parameters estimation. Additionally, they require high-frequency pulse width modulation and accurate voltage and current sensing [11,12]. The processing speed required to deal with this hardware-rich tasks reaches the order of microseconds to nanoseconds, as a result it becomes very complicated to implement within a DSPs or microprocessors software computation background. Additionally, the costs and complexity of these controllers are raised, due to the requirement of dedicated computers and specific integrated circuits. Similarly, dSPACE controller is also widely used in practice to achieve the control of power converters. Unfortunately it also has few drawbacks like need of additional software tools, requirement of dedicated computer and leads to high cost [13].

A hardware control solution using FPGA may solve the above problems. FPGAs are logic devices which contain a matrix of reconfigurable gate array logic circuitry. The use of FPGAs in low volume and high performance applications is very significant as it executes a lot of instructions in parallel which has lead them to be very powerful [14]. The main characteristic features of FPGAs are high processing speed, hardware programming flexibility and without changing the external circuitry, it is possible to reconfigure as per the requirement at a particular point of time [15]. These devices show greater potential for machine tool, solid state and deployed as controller for shunt/ series active filter, machine/ drive control, multilevel converters and chopper power circuits. Also, they are well-matched for manufacturing and automation environments [16].

The most attractive and highlighted feature in FPGAs is that they are programmed by utilizing Verilog HDL/VHDL (Hardware Description Languages (HDLs)) [17]. The advantage of using HDL is that it is technology independent and the software packages for these languages are freely available from Xilinx. The implementation of complex control designs on FPGAs is possible by defining hierarchical and modular description at various concept levels with the ultimate support of HDLs [13]. FPGAs utilize dedicated software and hardware for processing logic and it has a function of parallel processing, so they do not have a separate operating system [18]. A single FPGA controller is utilized to develop and implement the control algorithm for producing both low and high frequency switching pulses. The semiconductor switches available in hardware circuit is enabled by this switching pulses and to generate the preferred output signals [19].

Various current control methods are recommended for DSTATCOM configurations in the literature for generating the gate signals [20]. Based on that, hysteresis band current controller (HBCC) is highest efficient current control method compared to other current controllers. Owing to its advantages like high simplicity, good accuracy, outstanding robustness, fast dynamic response, current limiting capability and load time constant, it is mostly preferred and widely applied in DSTATCOM for compensating current related PQ problems. During the implementation it does not require complex processor. The switching pulses produced by HBCC module force the injected current to follow the reference compensator current. The primary feature of the HBCC is that it estimates the current error signals and directly generates the reference commands to the semiconductor switches present in the FL-DSTATCOM, when the error signals exceeds an assigned hysteresis band [21].

This paper expresses that the FPGA control of FL-DSTATCOM can be successfully implemented to enhance the quality of power distributed to consumers through 3-phase 4-wire EDS. The compensation capability of FL-DSTATCOM is verified under static, dynamic and combined loading conditions. Under static loading condition, the performance of FL-DSTATCOM is tested with unbalanced non-linear and unbalanced linear loads. Under dynamic loading condition, slip ring induction machine (SRIM) is considered and it is operated as motor to explore the dynamic reactive power support capability of FL-DSTATCOM. In the combined loading condition, the parallel combination of unbalanced non-linear load with slip ring induction machine is tested for harmonic current alleviation, compensation of reactive power and supply neutral current. The *d-q-0* components of load currents are utilized for generating compensator current for FL-DSTATCOM. The HBCC is utilized for producing the switching pulses required for eight semiconductor switches used in the FL-DSTATCOM. The various logic blocks of the synchronous reference frame theory (SRFT) control algorithm and HBCC has been programmed using Verilog HDL.

2. Implementation of FL-DSTATCOM and SRFT control algorithm

2.1. Experimental setup of FL-DSTATCOM

Fig. 1 shows the 3-phase power circuit schematic of FPGA controlled FL-DSTATCOM connected in a 4-wire 3-phase EDS. The laboratory prototype of FL-DSTATCOM is formed by connecting two 1-phase SEMIKRON make voltage source inverters (VSIs) (SKM150GB12T4) in parallel. In addition, SEMIKRON make 3000 μF/450 V (SKC 3M2-45A-3) DC bus capacitor is connected across them. The FL-DSTATCOM, which is usually a current controlled inverter, achieves NCC by fourth leg with less DC bus capacitor and therefore achieving full utilization of voltage across the DC capacitor. Remaining three legs present in the FL-DSTATCOM are used to compensate the reactive power, improve the power factor (PF), reduce the current harmonic and regulate the voltage.

The midpoint of each leg is coupled to the EDS through the 10 mH, 10 kHz, Ferrite core interface inductors which are used for proper shaping of the compensator current. The harmonic and reactive parts of load current are provided by FL-DSTATCOM so that the supply current contributes to only the active part of load current. The FL-DSTATCOM is controlled dynamically to maintain the supply side PF at unity under static, dynamic and combined loading conditions by maintaining the required voltage across the DC capacitor.

2.2. FPGA implementation of SRFT and HBCC

Reference compensating signal extraction and command signal generation for the FL-DSTATCOM are important stages of the control algorithm. Control strategy is the primary part of FL-DSTATCOM which substantially affects compensation characteristics. In the literature [22–24], several control algorithms were described for extracting the reference signal of DSTATCOM. Due to its greater accuracy, the SRFT algorithm is provided to be the most superior one. In this work, SRFT based algorithm is implemented for constructing reference compensator current using FPGA controller. The basic building blocks of SRFT based control algorithm for compensating static, dynamic and combined loads in EDS is depicted in Fig. 2. Also, the schematic shown in Fig. 3 designates the modular description of the control algorithm which includes

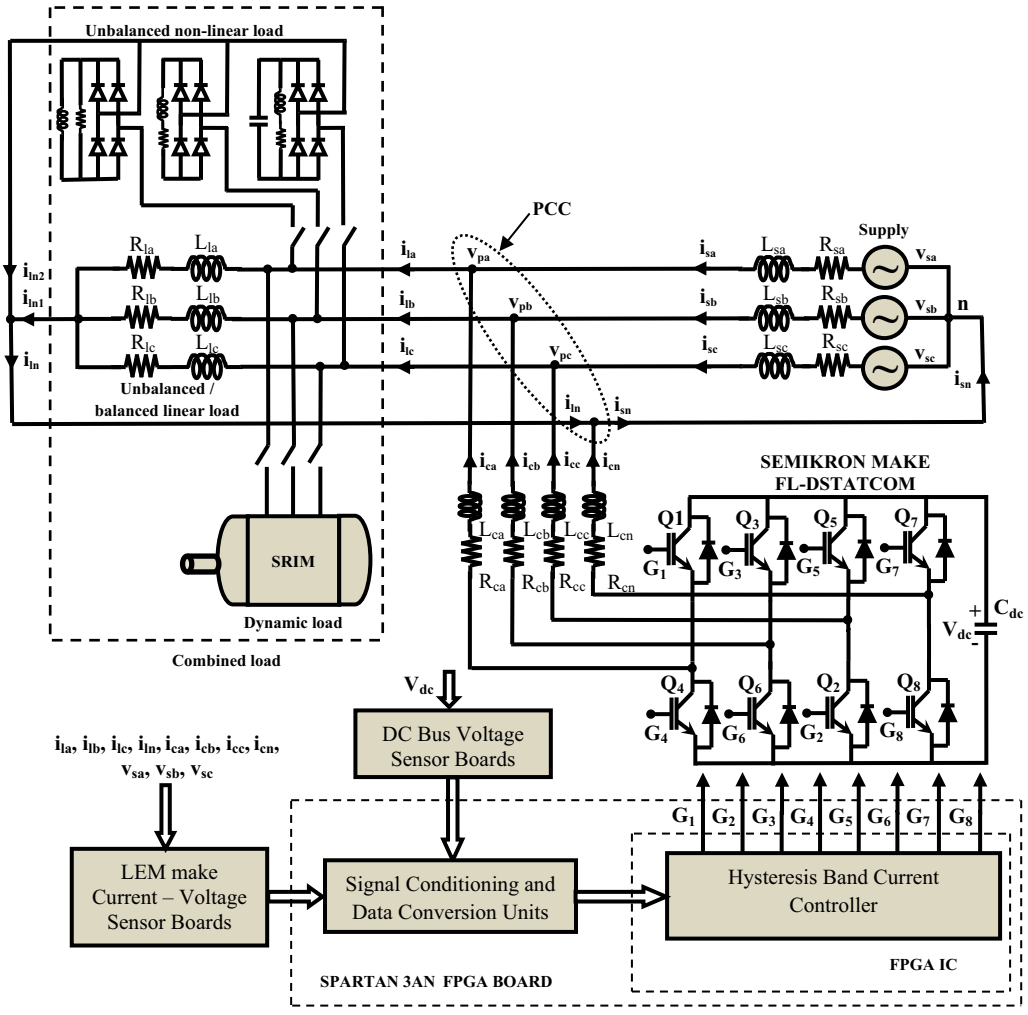

Fig. 1. Schematic of FPGA controlled FL-DSTATCOM.

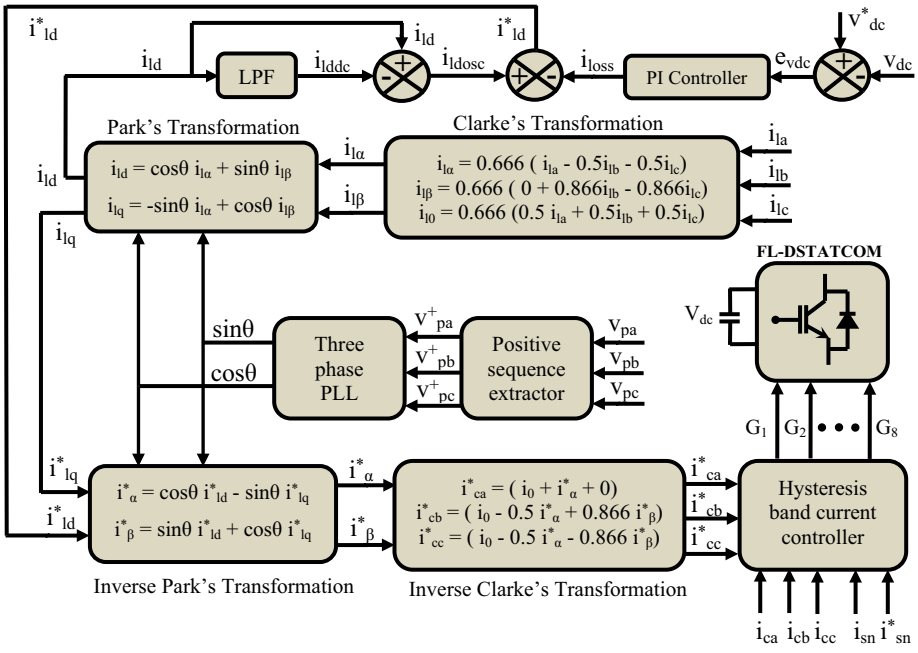

Fig. 2. SRFT control algorithm implemented in FPGA.

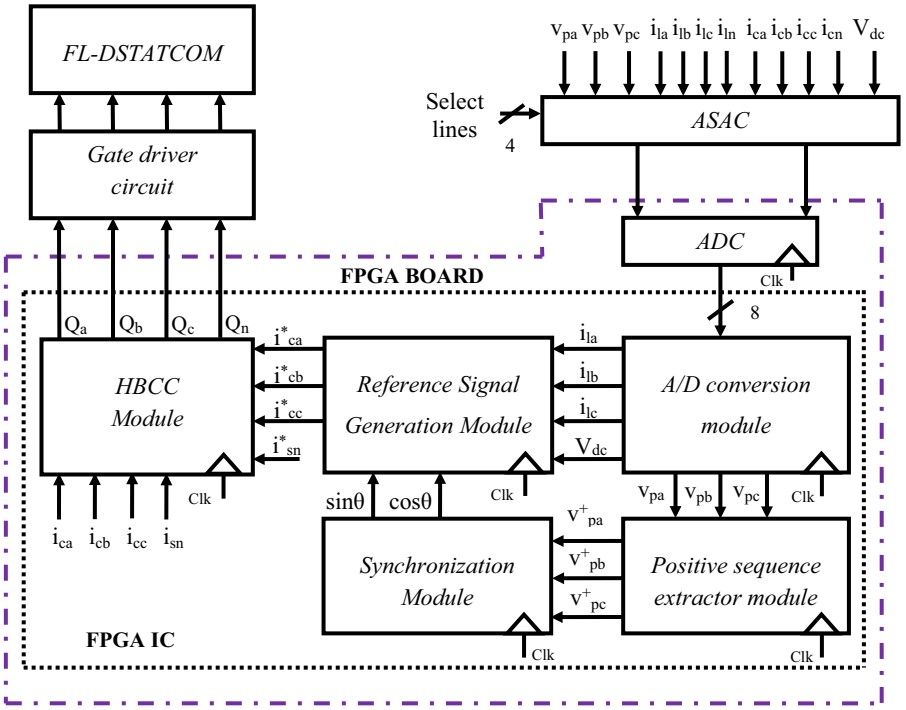

Fig. 3. Modular description of control strategy.

SRFT for reference current signal generation and HBCC for switching signals generation.

The control signals required to implement the modular design in FPGA are fed through analog signal acquisition card (ASAC). Once the required signals are readily available to FPGA, the modular design is implemented in five modules with the help of Altium design suite. The schematic shown in Fig. 4 is expressing the modular description of SRFT control algorithm and HBCC in Altium design suite. Current sensors (LEM make LA 55-P) and voltage sensor (LEM make LV 25-P) are used to sense the various current and voltage signals for the proper functioning of FL-DSTATCOM. The sensors are tuned so as its output voltage not to exceed the ADC voltage rating of the FPGA used for processing. The signals from the sensors are sent to analog multiplexer whose select line signals are controlled by FPGA.

2.2.1. Analog to digital conversion module

All the acquired analog signals are sent serially from multiplexer to the ADC module. This module converts the instantaneously varying analog values at high sampling rate to digital values for the processing in FPGA by receiving serial bits from the external ADC channel. The values are frequently updated for better performance. It deals with the synchronization of the external analog to digital converter with the FPGA and transfer the computed 8-bit data to the subsequent module. The 4 channel, 8 bit ADC084S021 device in Altium nano board NB3000XN is utilized for this research work. It is a low power converter with a high speed serial interface. It is powered from a regulated 3.3 V power supply and interfaces to the user FPGA over a serial peripheral interface (SPI) bus providing a sampling rate is the range of 50 ksps to 200 ksps. This module operates with a clock of 50 MHz.

This ADC module makes twelve conversions which include the 3-phase load current $i_{l(abc)}$ (i_{la}, i_{lb} and i_{lc}), load neutral current (i_{ln}), 3-phase compensator current $i_{c(abc)}$ (i_{ca}, i_{cb} and i_{cc}), compensator neutral current (i_{cn}), 3-phase PCC voltage $v_{p(abc)}$ (v_{pa}, v_{pb} and v_{pc}) and voltage across the DC capacitor (V_{dc}). The FPGA stores the digital values from the ADC module communicated serially in its registers and are frequently updated to its instantaneous values.

2.2.2. Positive sequence extractor module

To generate reference compensator current the synchronizing angle (cosθ and sinθ) is most essential one. This angle is evaluated with the help of positive sequence extractor block and 3-phase phase-locked loop (PLL). Hence the 3-phase PCC voltage ($v_{p(abc)}$) is fed as input to the positive sequence extractor module, where the PCC voltage is transformed into fundamental positive sequence voltage $v^{+}_{p(abc)}$ (v^{+}_{pa}, v^{+}_{pb} and v^{+}_{pc}) by executing the steps given in [25,26].

2.2.3. Synchronization module

This module receives the positive sequence component of 3-phase PCC voltage obtained from the previous module as input and provides the information regarding the synchronizing angle at its output. The 3-phase positive sequence voltages ($v^{+}_{p(abc)}$) are transformed into α-β coordinates (v_α and v_β) by using Eq. (1) and with the help of PLL, synchronizing angles (sinθ and cosθ) are obtained as follows:

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} v^{+}_{pa} \\ v^{+}_{pb} \\ v^{+}_{pc} \end{bmatrix} \tag{1}$$

$$\sin\theta = \frac{v_\alpha}{\sqrt{v_\alpha^2 + v_\beta^2}} \tag{2}$$

$$\cos\theta = \frac{v_\beta}{\sqrt{v_\alpha^2 + v_\beta^2}} \tag{3}$$

2.2.4. Reference signal generation module

This module generates the reference compensator current signals $i^{*}_{c(abc)}$ (i^{*}_{ca}, i^{*}_{cb}, and i^{*}_{cc}) for FL-DSTATCOM from $i_{l(abc)}$, synchroni-

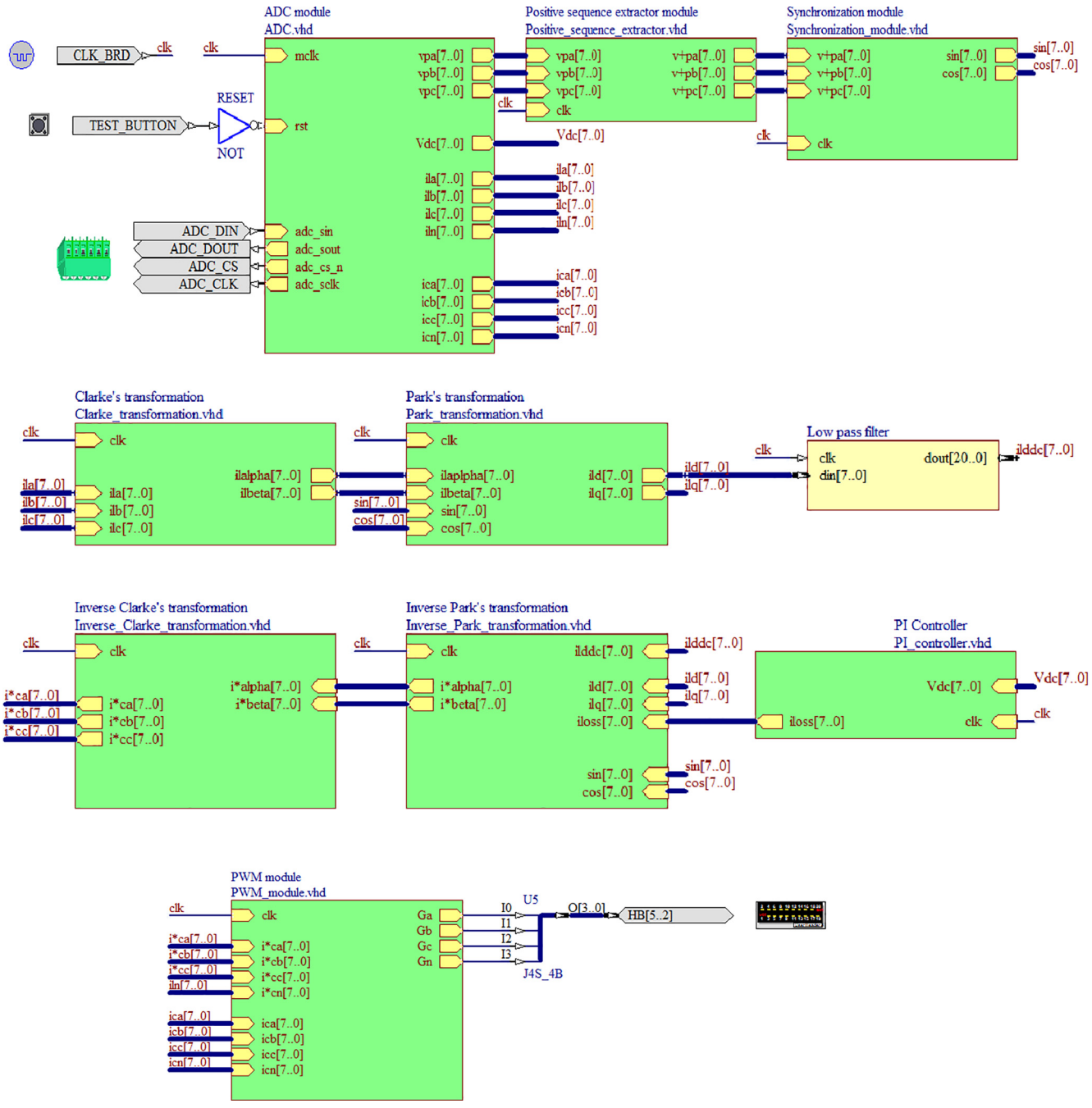

Fig. 4. Modular description of control strategy in Altium design suite.

sation angles, and V_{dc} as are inputs receiving from previous modules. As seen in Fig. 4 this module has Park's transformation and Clarke's transformation block, low pass filter (LPF), PI controller, reverse Park's transformation and Clarke's transformation block. The 3-phase load currents ($i_{l(abc)}$) are sensed and converted from *a-b-c* coordinate into stationary α-β coordinate using Clarke's transformation block. The *q*-axis component of the load current (i_{lq}) must be evaluated to estimate the requirement of load reactive power. The *q* component of the load current is utilized to generate reference supply current such that unity PF (UPF) is maintained at supply side. The *d-q* axis components corresponding to load current (i_{ld} and i_{lq}) in every phase are obtained using Park's transformation block. The DC component (i_{lddc}) of i_{ld} is extracted using digital LPF and it is deducted from i_{ld}, so that compensator delivers only oscillating part ($i_{ldosc} = (i_{ld} - i_{lddc})$) of the load active power and complete reactive power. The coefficients (0.104, 0.626, 0.626 and 0.104) for LPF are obtained using MATLAB toolbox. The error (e_{vdc}) between the set value of DC link voltage (V^*_{dc}) and the actual DC link voltage (V_{dc}) of FL-DSTATCOM is processed through a discrete PI controller to hold the DC capacitor voltage at a specified value which uses several registers to store the previous values and for compensating the power loss in the reactor, DC bus capacitor and switching devices. The oscillating part of i_{ld} is combined with the output of PI controller representing the power loss (i_{loss}) to obtain reference *d*-axis current ($i^*_{ld} = (i_{ldosc} - i_{loss})$). Then reference *d*-axis current i^*_{ld}, which in conjunction with i_{lq} are translated to *a-b-c* frame using reverse Park's transformation and Clarke's transformation to obtain the reference compensator current $i^*_{c(abc)}$ for FL-DSTATCOM.

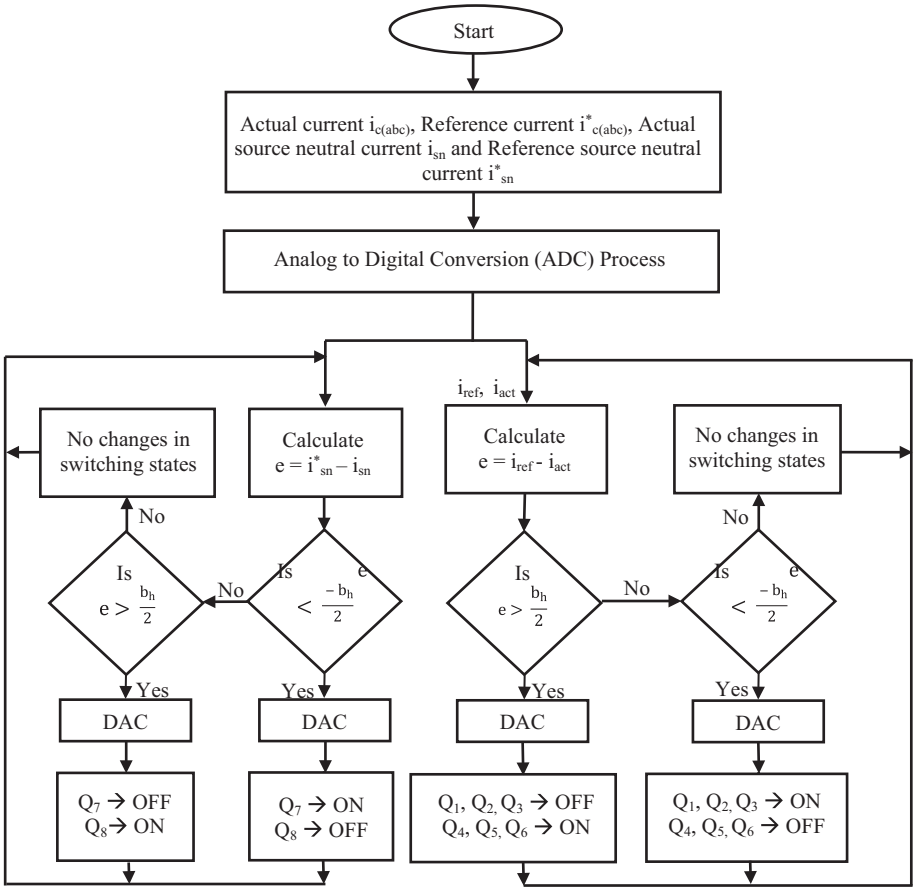

Fig. 5. Flow chart for switching logic.

2.2.5. HBCC module

Then the reference current ($i_{ref} = i^*_{c(abc)}$) and the sensed FL-DSTATCOM current ($i_{act} = i_{c(abc)}$) are fed as input to the HBCC block as shown in Fig. 4. Switching pulses produced by HBCC module forces the injected current close to the reference compensator current. The flow chart for switching logic shown in Fig. 5 has been effectively utilized for producing switching pulses for FL-DSTATCOM, where b_h is the hysteresis band of reference compensator current.

If the injected current (i_{act}) is higher than the reference current (i_{ref}) (i.e.) (i_{act}) $\geq$ ($i_{ref} + b_h/2$), Q_1, Q_3 and Q_5 are turned OFF, and Q_2, Q_4 and Q_6 are turned ON. If the compensator current is smaller than the reference current (i.e.) (i_{act}) $\leq$ ($i_{ref} - b_h/2$), Q_1, Q_3 and Q_5 are turned ON, and Q_2, Q_4 and Q_6 are turned OFF. If the injected current is within limits, (i.e.) ($i_{ref} - b_h/2$) $\leq$ (i_{act}) $\leq$ ($i_{ref} + b_h/2$), than no change is done in the switching pulses. Based on the above logic, the gate signals are generated for six power semiconductor switches present in the VSI. A negative addition of 3-phase supply currents $i_{s(abc)}$ (i_{sa}, i_{sb} and i_{sc}) is considered as supply neutral current ($i_{sn} = -(i_{sa} + i_{sb} + i_{sc})$). This current is compared with the reference supply neutral current ($i^*_{sn} = i^*_0 = 0$), and the current error is utilized to produce the switching signals for switches Q_7 and Q_8 present in FL-DSTATCOM within HBCC module to compensate the supply neutral current. Finally, the generated gate pulses are fed to gate driver circuit (HCPL3101) for voltage and current boosting. These gate signals are then applied to the IGBTs in the power circuit. The device utility summary produced by the Altium design suite is depicted in Fig. 6.

3. Performance evaluation

A 4-wire 3-phase FL-DSTATCOM circuit shown in Fig. 1 has been built in the hybrid electrical systems (HES) laboratory which is shown in Fig. 7 for compensating multifarious loads. The experimental setup parameters of system under study are presented in Table 1.

The SRFT based control algorithm and HBCC is fully programmed in Verilog HDL, implemented using Altium design suite and finally loaded into the SPARTAN 3AN FPGA. The sampling frequency is 20 kHz. For recording the experimental results on the implemented prototype of FL-DSTATCOM during evaluation, an advanced PQ analyzer (Fluke 430-II) and a 4-channel digital storage oscilloscope (DSO-X-2014A) are used. The performance behaviour of FL-DSTATCOM for compensating unbalanced non-linear/linear load, dynamic load and combined loads are discussed in the following section.

3.1. Compensation behaviour of FL-DSTATCOM for static loads

3.1.1. Compensation of neutral current and harmonic alleviation

The behavior of FL-DSTATCOM during unbalanced non-linear loading is presented in Fig. 8. The 3-phase unbalanced non-linear load is composed by three 1-phase diode bridge rectifier followed by R-L load. The waveforms of phase-a supply current (i_{sa}) and voltage (v_{sa}) without FL-DSTATCOM are plotted in Fig. 8a. The supply current is same as the load current, unbalanced, contains harmonics and lags the voltage. The Fig. 8b indicates the waveforms of phase-a supply current and voltage with FL-DSTATCOM.

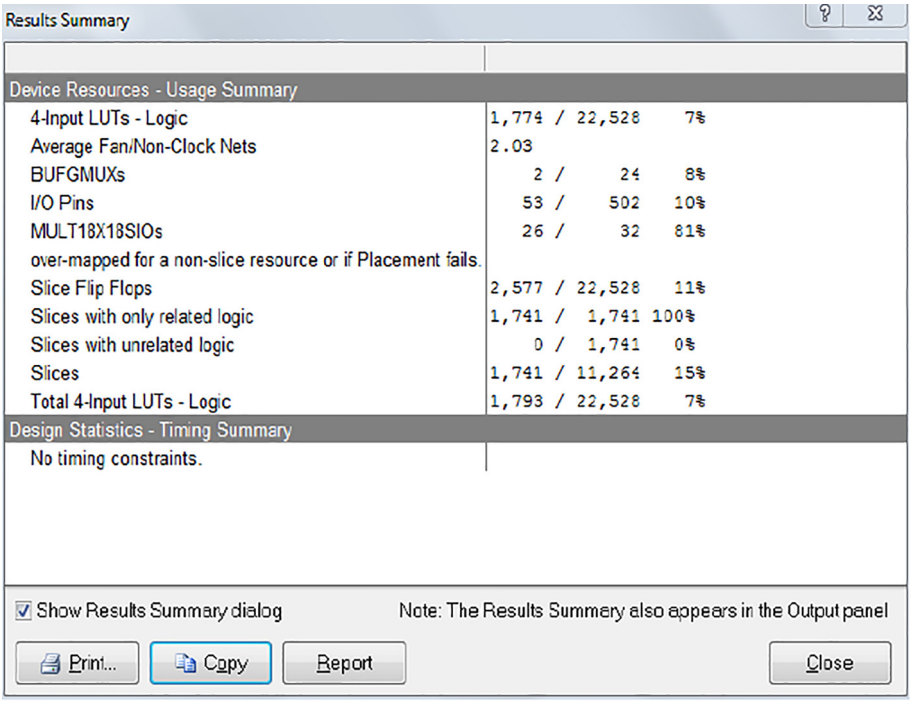

Fig. 6. Resource utilization in FPGA.

Fig. 7. Snap shot of the implemented FL-DSTATCOM in the HES laboratory. (1) 3-phase supply (2) Feeder (3) Signal conditioning and acquisition circuit (4) PCC (5) Fluke meter (6) DSO (7) Load switch (8) Static load (9) RC filter (10) RL filter (11) FL-DSTATCOM (12) Gate driver circuit (13) FPGA board (14) Dynamic load (SRIM) (15) DC machine.

The unbalanced supply current is converted into balanced sinusoidal supply current and it is in-phase with voltage. The current harmonics present in the supply current is shown in Fig. 8c. It has a total harmonic distortion (THD) of 19.6% without FL-DSTATCOM. Due to the proper control of FPGA based FL-DSTATCOM, the supply current is shaped into sinusoidal. Further, %THD of the supply current is decreased to 4.5% which can be observed from Fig. 8d. Due to the nature of unbalanced non-linear load, some finite amount of current flows in the neutral conductor which is shown in Fig. 8e. Fig. 8f indicates that the fourth leg of FL-DSTATCOM forces the supply neutral current to zero.

3.1.2. Compensation of load reactive power and supply neutral current

The behaviour of FL-DSTATCOM during unbalanced linear loading is presented in Fig. 9. Without FL-DSTATCOM, the supply currents are unbalanced and are not in-phase with the voltage. After connecting FL-DSTATCOM, it starts to compensate the unbalanced supply current with the help of reference current computed using FPGA controller and maintains the supply current as balanced and also in-phase with the voltage, which can be clearly observed in Fig. 9a and Fig. 9b.

From Fig. 9c and Fig. 9d, it is evident that the supply reactive power (Q) is reduced to 30 VAr from 300 VAr and the PF at supply

Table 1
Design specifications for experimental studies.

Component	Value
Supply voltage	75 V (Ph-n), 50 Hz
Feeder	R_s = 5 Ω/phase L_s =6 mH/phase (Iron core, 50 Hz)
Filter	R_f = 2 Ω/phase L_f = 10 mH/phase (Ferrite core, 10 kHz)
Unbalanced R-L Load	Za = 30 + j25.13 Ω; Zb = 50 + j31.41 Ω; Zc = 40 + j18.84 Ω
Unbalanced non-linear load (Three 1-phase rectifiers supplying R-L load)	Za = 30 + j25.13 Ω; Zb = 50 + j31.41 Ω; Zc = 40 + j18.84 Ω
Voltage Source Inverter	C_{dc} = 3000 μF, V_{dc} = 180 V
HBCC	b_h = 0.2 A
Gain of DC capacitor voltage controller	K_p = 0.6, K_i = 1.19

side improved from 0.66 to 0.91 lag. Thus, the compensation of reactive power is realized by FL-DSTATCOM and also the supply side PF is improved to unity. It is seen from Fig. 9e and Fig. 9f that due to the presence of fourth leg of the FL-DSTATCOM, current in the neutral conductor is decreases to zero A.

3.2. Compensation behaviour of FL-DSTATCOM for dynamic loads

Under various loading conditions, the capability of FL-DSTATCOM for compensation of dynamic reactive power demand of a slip ring induction motor is verified with the help of SRFT based control technique using FPGA controller. The slip ring induction motor used in the HES laboratory prototype is a 3 HP 4 pole 50 Hz machine and is fed with 200 V (L-L) during experimentation. Fig. 10a and Fig. 10b presents the plots of phase-a supply voltage and current without and with FL-DSTATCOM. In these plots, without FL-DSTATCOM, supply current lags the voltage, which confirms that the induction motor is demanding reactive power from the

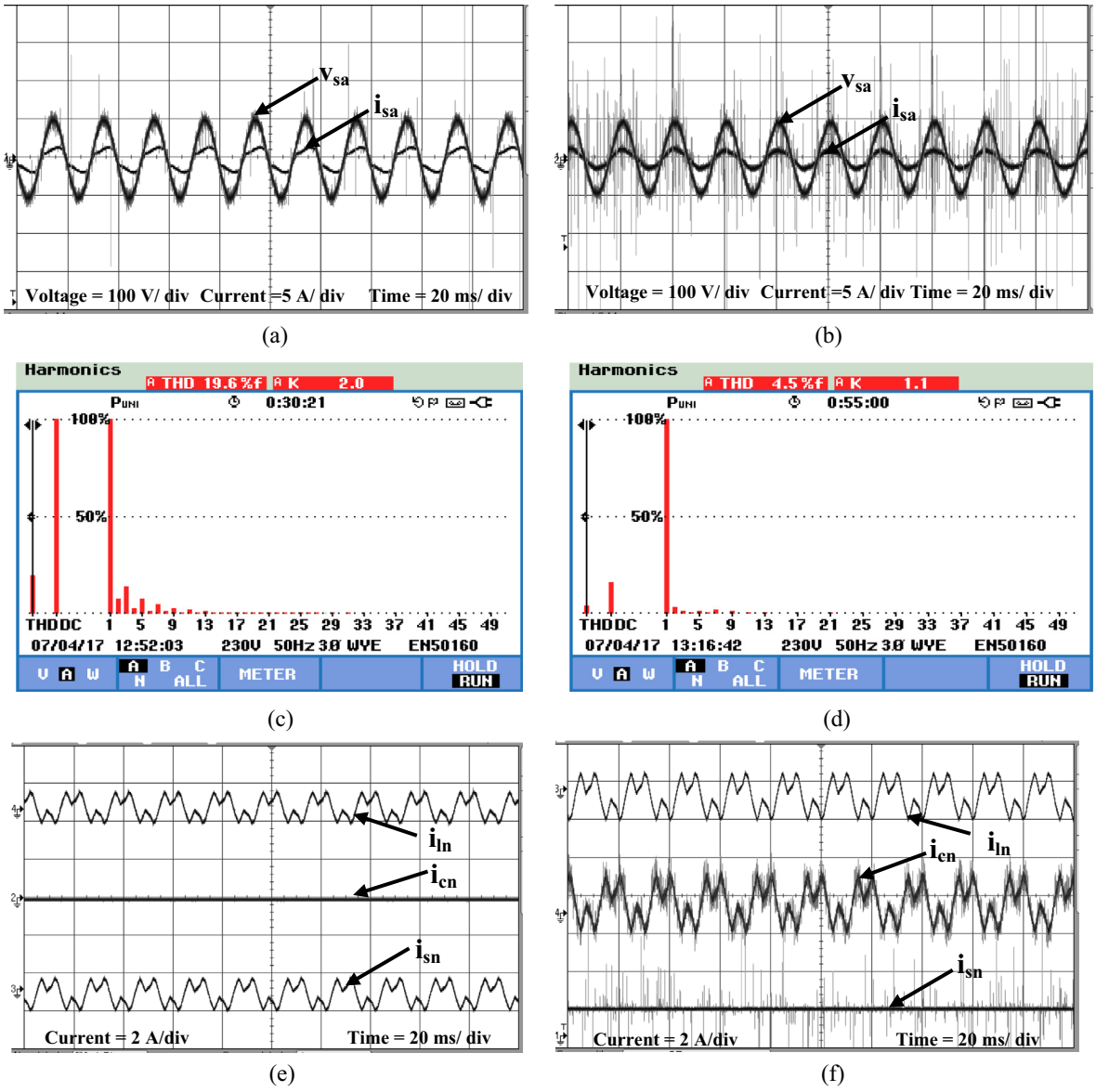

Fig. 8. Waveforms showing compensation of supply neutral current and harmonic alleviation (a) v_{sa} and i_{sa} without FL-DSTATCOM (b) v_{sa} and i_{sa} with FL-DSTATCOM (c) Harmonic spectrum of i_{sa} without FL-DSTATCOM (d) Harmonic spectrum of i_{sa} with FL-DSTATCOM (e) Current in the neutral (load (i_{ln}), compensator (i_{cn}) and supply (i_{sn})) without FL-DSTATCOM (f) Current in the neutral with FL-DSTATCOM.

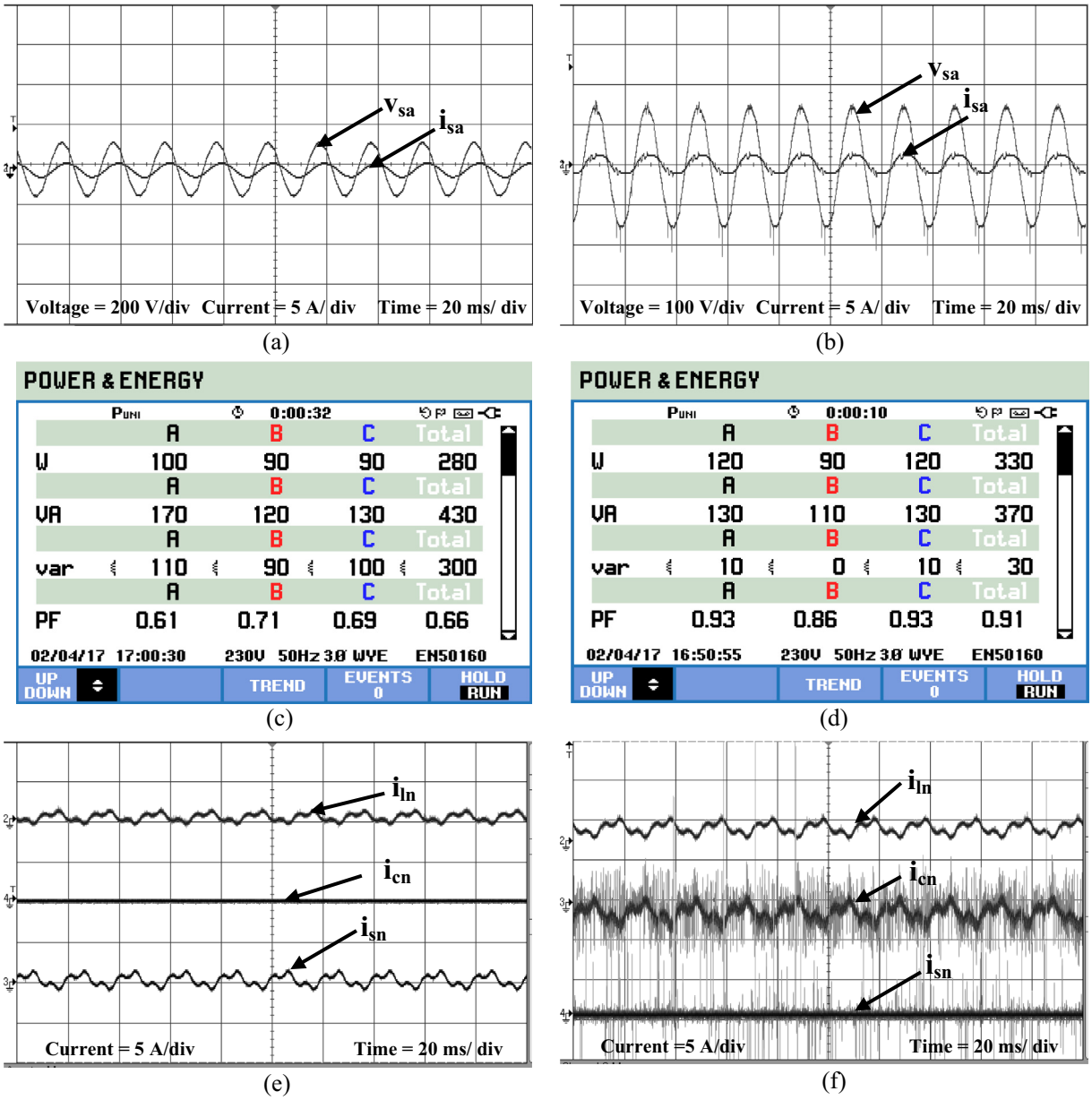

Fig. 9. Waveforms showing neutral current and reactive power compensation. (a) v_{sa} and i_{sa} without FL-DSTATCOM (b) v_{sa} and i_{sa} with FL-DSTATCOM (c) P and Q without FL-DSTATCOM (d) P and Q with FL-DSTATCOM (e) Neutral current without FL-DSTATCOM (f) Neutral current with FL-DSTATCOM.

supply. After the connection of FL-DSTATCOM, the reactive power demanded by the slip ring induction motor is provided by the compensator leading to UPF operation at the supply side. The active and reactive powers drawn by the motor at a load current of 1.75 A from the grid before and after connecting the compensator are depicted in Fig. 10c and 10d respectively. After connecting the compensator, the reactive power drawn from the grid decreases to 90 VAr from 810 VAr and also the PF at supply side improved from 0.56 to 0.96 lag. It can be further noticed that there is a rise in active power (P) when the compensator is turned ON, which is mainly for feeding the inverter losses and maintaining DC capacitor voltage constant.

The capability of FL-DSTATCOM for catering dynamic reactive power compensation and PF improvement under different load current is shown in Fig. 11 and Fig. 12. It can be clearly observed that the difference in active power drawn from the grid without and with compensator, which corresponds to the inverter power loss, is nearly constant during all loading conditions.

3.3. Compensation behaviour of FL-DSTATCOM for combined load

The hardware results during the behaviour of FL-DSTATCOM in this test case are presented in Fig. 13. In this case, unbalanced nonlinear loads are operated in parallel with slip ring induction motor. Without FL-DSTATCOM, the supply currents are unbalanced and non-sinusoidal. It consists of harmonics and lags the supply voltage. During this period, combined load is drawing reactive power from the grid. After the connection of compensator, the FL-DSTATCOM instantly starts its performance and converts the unbalanced supply current into balanced and sinusoidal. Moreover the supply current is made in-phase with voltage, which is depicted in Fig. 13a and b. The unbalanced non-sinusoidal supply current has a THD of 17.9%. After connecting the FL-DSTATCOM,% THD of the compensated supply current decreased to 3.9% which is clearly seen from Fig. 13c and d.

The complete reactive power demand of combined load is met by compensator and hence the supply side reactive power reduces

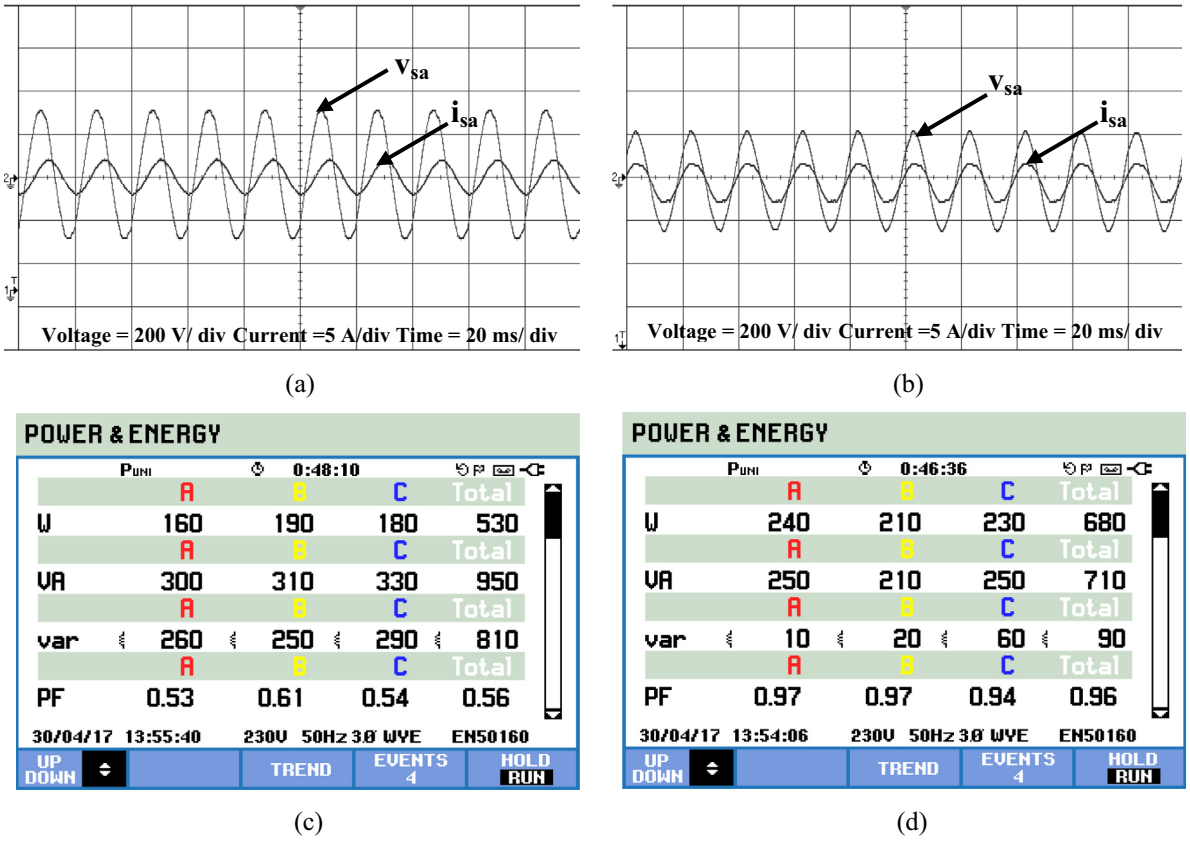

Fig. 10. Waveforms showing compensation of reactive power of slip ring induction motor. (a) v_{sa} and i_{sa} without FL-DSTATCOM (b) v_{sa} and i_{sa} with FL-DSTATCOM (c) P and Q without FL-DSTATCOM (d) P and Q with FL-DSTATCOM.

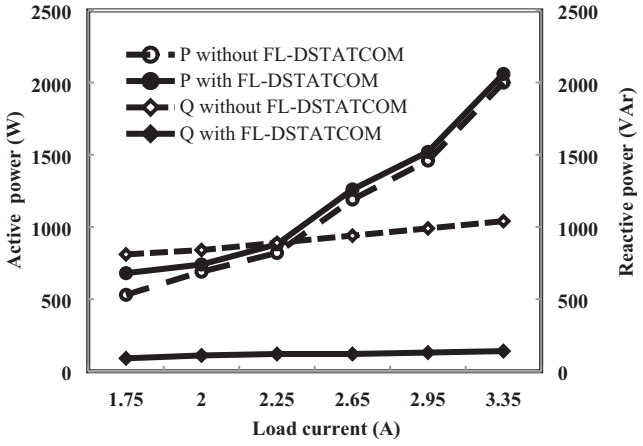

Fig. 11. P and Q support by the supply under dynamic loading.

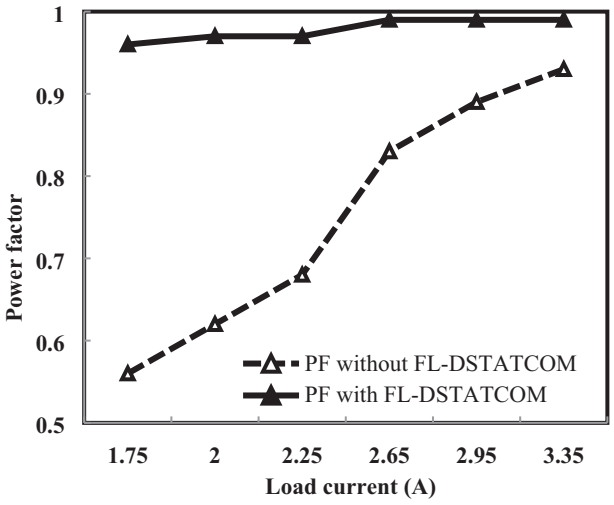

Fig. 12. Power factor improvement during dynamic loading.

from 370 VAr to 60 VAr leading to nearly UPF operation at the supply side as indicated in Fig. 13e and f. It is seen from Fig. 13g and h that due to the presence of fourth leg of the FL-DSTATCOM, neutral current of supply decreases to zero.

4. Conclusion

In this paper, the compensation behaviour of four-leg distribution static compensator (FL-DSTATCOM) under static, dynamic and combined loading conditions has been illustrated through FPGA based system experimentation results. Under static loading condition the practicability of FL-DSTATCOM is analysed for load balancing, neutral current reduction, reactive power support and harmonic alleviation. Additionally, the effectiveness of dynamic compensation by FL-DSTATCOM is examined with grid connected slip ring induction machine in motoring mode. Further, in combined loading condition, the composite compensation capability of FL-DSTATCOM is confirmed. The SRFT control algorithm and HBCC technique have been effectively implemented with a modular design approach, in which each task of control algorithm has been built on FPGA using Verilog HDL coding. Before compensation, all phases in the supply end exhibit a lagging power factor

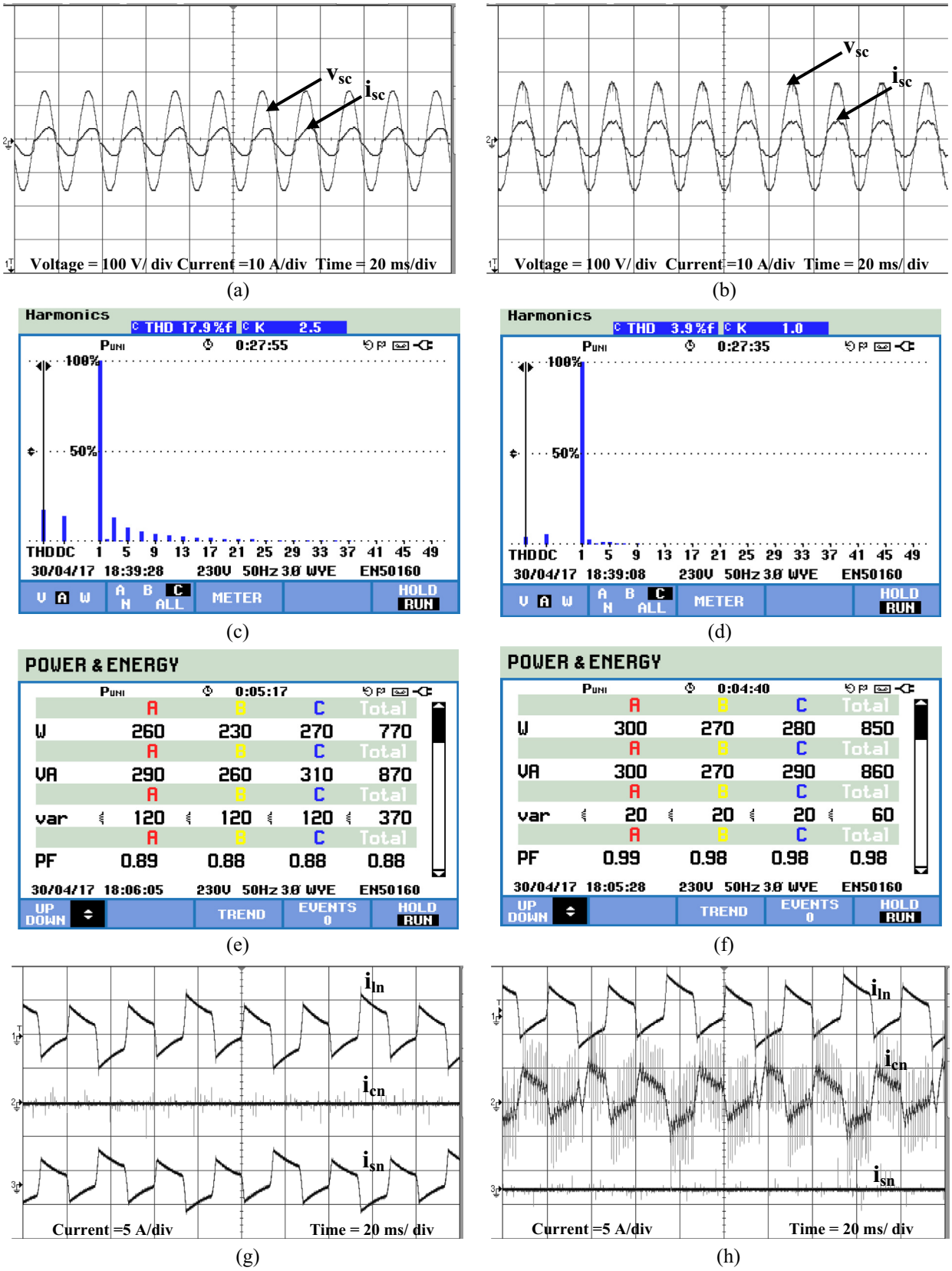

Fig. 13. Waveforms during compensation of supply neutral current, reactive power and harmonics for combined load (a) v_{sc} and i_{sc} without FL-DSTATCOM (b) v_{sc} and i_{sc} with FL-DSTATCOM (c) Harmonic spectrum of i_{sc} without FL-DSTATCOM (d) Harmonic spectrum of i_{sc} with FL-DSTATCOM (e) P and Q provided by supply without FL-DSTATCOM (f) P and Q provided by supply with FL-DSTATCOM (g) Current in the neutral without FL-DSTATCOM (h) Current in the neutral with FL-DSTATCOM.

which indicates that reactive power demand is fed by the supply. After compensation, with the help of FPGA controlled FL-DSTATCOM, UPF is maintained at the supply end which indicates the satisfactory performance of SRFT algorithm based FL-DSTATCOM. Especially, the current in the neutral conductor is effectively nullified with the help of fourth leg of FL-DSTATCOM under unbalanced and combined loading conditions. %THD of supply current is reduced in compliance with IEEE-519 standards. Based on the extensive experimentation study carried out in this work and the results obtained with multifarious loading conditions, the FPGA controlled FL-DSTATCOM is found to be offering excellent performance comparable with the other advanced digital controllers like DSP, microprocessors. The FPGA controller is capable of functioning without a dedicated PC which is mandatory for a dSPACE controller.

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