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MEMS Scale CMOS Compatible Energy Harvesters Using Piezoelectric Polymers for Sustainable Electronics

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MEMS SCALE CMOS COMPATIBLE ENERGY HARVESTERS USING PIEZOELECTRIC POLYMERS FOR SUSTAINABLE ELECTRONICS

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MEMS Scale CMOS Compatible Energy Harvesters Using Piezoelectric Polymers for Sustainable Electronics (August 2017)

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The field of microelectronics had a remarkable progress since its beginnings in 1960s, which led to the advent of myriad new electronic devices that found widespread usage in daily life. Continuous advances in CMOS and MEMS technologies reduced the cost, size, weight, and power requirements of these devices, enabling the realization of distributed systems such as wireless sensor networks. However, due to much slower pace of innovation, currently available battery technologies continue to dictate the size, weight and cost of these systems. There are further concerns brought by the batteries regarding the environmental effects or feasibility of dead battery replacement in distributed or embedded systems. As a result of this problem, there has been a growing research impetus on energy harvesting technologies, which are expected to alleviate the problems brought by the fixed capacity energy sources in electronic devices.

This dissertation proposes a new class of MEMS-scale piezoelectric energy harvesters that have the potential to be monolithically integrated with CMOS circuits. Proposed devices will utilize polyvinylidene fluoride-trifluoroethylene (PVDF-TrFE), a piezoelectric polymer with an impressive electromechanical coupling factor of 0.3. Its energy harvesting potential was evaluated using theoretical analyses and finite element method (FEM) simulations and compared with other CMOS compatible piezoelectric

materials. Various architectural options for the mechanical and electrical structure of the energy harvester were examined and most promising options were determined.

The process for the fabrication of PVDF-TrFE thin films was optimized to yield high quality films with strong ferroelectric and piezoelectric properties. A comprehensive characterization study was performed to measure the dielectric, ferroelectric, and piezoelectric properties of the fabricated films. Cantilever type MEMS scale piezoelectric energy harvesters (PEH) were fabricated and characterized. Maximum power output density on purely resistive loads in response to a 1.0 g input acceleration was measured as 27.8 nW/mm^2 from a (1800 μm × 2000 μm) device at its resonance frequency of 192.5 Hz. A power conditioning circuit, based on synchronous switching on inductor technique, was also designed and integrated with the fabricated prototypes. The circuit, which draws 250 nW power from ±1 V dual supplies at 200 Hz, improved the DC power output of the PEHs by 165%. Using the same (1800 μm × 2000 μm) prototype in combination with the circuit, a maximum power of 140 nW was transferred to a DC load under 1.0 g acceleration.

The results obtained throughout the course of this dissertation work proved that PVDF-TrFE can be used in MEMS scale energy harvesting devices. CMOS compatible fabrication process of the polymer makes it possible to integrate these energy harvesters with CMOS circuits on the same substrate. This monolithic integration approach would improve the unit cost, size, and reliability compared to integration at higher levels and therefore, can find use in applications such as wireless sensors networks, structure health monitoring systems, and wide area surveillance applications.

Dedicated to the memory of my father,

Mustafa Toprak

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TABLE OF CONTENTS

Page

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1: INTRODUCTION

The advent and subsequent rapid progress of microelectronics had a revolutionary effect on human civilization in the last five decades. Mass fabrication of highly integrated smart electronic devices such as sensors, actuators, transmitters, receivers, and processors led to the emergence of myriad applications that facilitated daily life. Concurrent advances in complementary metal oxide semiconductor (CMOS) and microelectromechanical systems (MEMS) technologies improved the performance of these devices while reducing their dimensions, costs, and power requirements. The ongoing trend for smaller and cheaper devices, combined with the improvements in wireless communication capability, enabled the realization of distributed systems such as wireless sensor networks (WSN). However, the success of these nascent technologies depends on the availability of reliable energy sources. Fixed capacity energy sources such as batteries give rise to cost, size, and lifetime problems. *The basis of this dissertation is energy harvesting, which is an alternative solution that can address these problems.*

1.1 Energy Harvesting Overview

Energy harvesting can be simply defined as converting otherwise unused energy available in the environment into electrical energy for immediate or later use. Electrical energy is one of the most prominent commodities of the modern world; consequently, there are a great number of applications where energy harvesting devices can be utilized. The main factor that determines the potential applications is the scale of the harvestable energy. Large scale energy sources such as ocean waves or bridge vibrations can be utilized to support power grids as clean, renewable energy sources [1]. At smaller scales,

available energy is more suitable for powering standalone electronic sensors and transducers, which is typically done by batteries in current technology examples.

There are various energy sources available in the environment that can be harvested, including solar energy, structural vibrations, radio frequency (RF) waves, acoustic waves, and temperature gradients [2]. Among these potential sources, solar energy can provide the highest power density under direct sunlight [3]. However, this density drastically drops in a dim environment. Furthermore, transparency requirement renders solar energy harvesting useless in implanted or embedded systems. In comparison, mechanical vibrations can provide a power density level similar to solar energy in a cloudy environment [3]. In addition to this relatively high power density level, an important advantage of the vibration energy harvesting is the sturdy nature of its energy coupling mechanism. Unlike sunlight, vibrations cannot be easily absorbed or reflected by the materials on their propagation paths; in fact, specially designed vibration isolation systems are required to eliminate vibration coupling in sensitive applications such as atomic force microscopy (AFM). This usually unwanted phenomenon makes vibration energy harvesting a more versatile method that can be used in implanted or embedded systems.

There are a variety of vibration sources, especially in urban environment, generating vibrations with different amplitudes and frequencies. The range of the amplitude and frequencies vary from 4 m/s^2 at 1 Hz for a walking human to 20 m/s^2 at 44 Hz for an air compressor. [2-4]. Mechanical vibrations can be converted into electrical energy by coupling these vibrations onto a proof mass and then extracting its kinetic energy. The energy extraction can be done via electromagnetic, electrostatic, or piezoelectric

mechanisms [5]. Among these three methods, piezoelectric energy harvesters (PEH) have been reported to have higher energy density values [5, 6]. Higher energy density of PEHs become more pronounced in smaller scales; output power level of piezoelectric and electromagnetic harvesters scale with $V^{4/3}$and V^2, respectively, where V is the effective material volume [7]. In addition to the higher energy density, PEHs have the advantage of architectural simplicity. Piezoelectric materials have an inherent reciprocal energy conversion capability between mechanical and electrical domains. This inherent conversion mechanism eliminates the need for any extra inputs, such as an external magnetic field or voltage source. Simple architecture is a key advantage in small scale devices where assembling individual components is simply not feasible and microfabrication techniques are utilized. There are several piezoelectric materials that can be utilized via microfabrication techniques. Due to these most salient advantages, PEHs are the most prominent candidates to supply energy for small scale devices.

1.2 Piezoelectric Energy Harvesters

It is possible to use different criteria to classify PEHs, such as the type of the harvested energy, target application, mechanical architecture, and device dimensions. In this section, a brief literature survey of PEHs classified into three groups according to device dimensions is presented. These three groups are (i) macro/meso-scale, (ii) MEMS-scale, and (iii) nano-scale PEHs. The distinction between meso-scale and MEMS scale devices is made according to the fabrication method rather than dimensions; manually assembled devices are classified as meso-scale, whereas devices fabricated using lithography and microfabrication techniques are classified as MEMS-scale [8]. Nano-scale group includes only PEHs constructed using piezoelectric nanowires.

1.1.1 Macro and Meso-Scale Piezoelectric Energy Harvesters

Current research on energy harvesting is mostly focused on smaller scale devices that can provide enough energy to create autonomous nodes for distributed systems such as WSNs. Nevertheless, there have been efforts to use PEHs as a clean energy source to support the existing power grid. A consultant report prepared for California Energy Commission in 2013 evaluated the feasibility of this approach and concluded that more comprehensive tests are necessary [9]. Considering the high costs associated with large scale energy projects, it is unlikely that large scale piezoelectric energy harvesting will have widespread implementation in the near future.

Meso-scale PEHs, manually assembled PEHs with dimensions ranging from a few millimeters to several centimeters, can be used to supply power for WSNs or IMDs. The first examples of meso-scale PEHs were proposed in 1960s as a permanent power supply for the pacemakers, a relatively new technology at the time [10, 11]. Another device for the same purpose was proposed by Hasler et al. in 1984 [12]. After these implantable devices, Antaki et al. proposed a shoe-embedded PEH to provide power for medical implants in 1995 [13]. In similar studies on harvesting power from human gait, the utilization of harvested energy was demonstrated by intermittently operating a radio frequency identification (RFID) tag [14, 15]. The idea to use PEHs to charge batteries came to light as personal portable electronic devices such as cell phones and laptops gained widespread use. In 1996, Umeda et al. investigated the feasibility of harvesting mechanical impact energy using PEHs for this purpose [16, 17].

These early studies on PEHs investigated the possibility of harvesting energy from direct mechanical forces such as arterial pressure or heel strikes. Another possible energy

source that can be exploited via piezoelectric energy harvesting is mechanical vibrations. Vibration energy harvesting with PEHs is performed by converting the periodic motion of a proof mass into mechanical stress in the piezoelectric material. The typical mechanical structure used for this purpose is the cantilever beam [6, 18-20].

Piezoelectric materials can also be used to harvest energy from varying pressure fields; but this necessitates physical separation of the medium in order to accommodate a pressure difference acting on the PEH. Mechanics of pressure mode energy harvesting using diaphragms have been studied theoretically and experimentally [21-25]. Piezoelectric diaphragms have also been proposed to harvest energy from vibrations in a number of studies [26-28]. However, significantly high stiffness of a diaphragm compared to a similar sized cantilever leads to higher resonance frequencies.

Most PEHs utilize mechanically compliant structures such as cantilevers or diaphragms. It is also possible to harvest energy using bulk piezoelectric materials; however, this approach requires higher input forces to induce same strain levels due to the typically high bulk moduli. Nevertheless, significantly increased piezoelectric material volume makes it an attractive alternative when high forces are available. Some researchers used force amplifiers coupled to thick piezoelectric disks or blocks to increase harvested energy [29, 30]. Utilization of piezoelectric actuator stack for energy harvesting was also demonstrated with [31] and without [32] mechanical force amplifiers.

1.1.2 MEMS Scale Piezoelectric Energy Harvesters

Microfabrication techniques have remarkably improved since their emergence with the advent of microelectronics. These improvements have been mostly driven by the demand from complementary metal oxide semiconductor (CMOS) and

microelectromechanical systems (MEMS) markets. CMOS and MEMS technologies enabled the mass fabrication of small-size integrated transducers on inexpensive silicon substrates at very low unit costs. As a result, these miniature electronic transducers have become ubiquitous and myriad trends started to emerge such as smart-home sensors, implantable medical devices (IMD), and WSNs. Driven by these trends, there have been a remarkable number of studies on MEMS scale PEHs in the last decade. Embedded MEMS-scale PEHs can supply part of the required energy during transducer operation or can be used to recharge the batteries, leading to smaller or longer lasting batteries. One of the most prominent challenges of MEMS-scale PEHs is the attainable output power levels, which is limited due to small device volume. This problem is aggravated by fabrication and material limitations. Microfabricated PEHs are in unimorph configuration since the devices can be fabricated on only one side of the substrate [33]. Furthermore, electromechanical conversion efficiency of thin film piezoelectric materials are lower compared to their bulk counterparts [34]. Another challenge in the design of MEMS scale resonant mode PEHs is the high resonance frequencies, which is caused by increased mechanical stiffness and reduced equivalent mass as the dimensions get smaller. On the other hand, as the power requirements of transducers are being continuously reduced by shrinking transistor dimensions and innovative circuit architectures, even microwatt-level powers are becoming a significant contribution. The ultimate goal in this realm would be to completely eliminate the need for batteries by increasing the harvested energy levels above the requirements of the transducer.

Lead zirconium titanate (PZT) is probably the most commonly preferred piezoelectric material in MEMS scale PEHs since it can be deposited as thin film layers

and exhibits remarkably strong piezoelectric properties. The first study reporting a fully microfabricated PEH was published by Jeon et al. in 2003 [35]. The 170 μm-long prototype cantilever utilizing a PZT thin film coated on a SiO_2 structural layer harvested 1 μW power from a 10.9g input acceleration at 13.7 kHz. [35]. The authors improved this prototype in later studies by reducing the cantilever bending induced by residual stresses of thin film layers [36, 37]. Another MEMS scale cantilever type PEH utilizing thin film PZT was reported by Fang et al. in 2006 [38]. Their device had a much lower resonance frequency, 609 Hz, due to the 0.15 mm^3 Ni proof mass formed using UV-LIGA technique [38].

The sol-gel method used to coat the PZT thin films in these studies has certain advantages such as precise composition control ability, high film quality, and relatively low cost [39]. Consequently, it is a widely preferred method for PZT based MEMS scale PEHs [40-42]. On the other hand, the thickness of each layer that can be coated without crack formation is limited in this method; and therefore, even sub-micron films are coated in several steps [37-39]. This makes it impractical to fabricate sol-gel PZT layers thicker than a few microns. As a solution to this problem, Lee et al. designed an aerosol PZT deposition system with a deposition rate capability of 0.1 μm/min [43]. Using their aerosol deposition system, they fabricated cantilever type energy harvesters with 5 μm-thick PZT layers [44]. However, the remnant polarization of their PZT film was measured as 7.3 – 9.0 $\mu C/cm^2$, which is lower than the values obtained from sol-gel films [38, 40]. As a matter of fact, even the better quality sol-gel thin films have considerably lower electromechanical coupling coefficients compared to bulk PZT ceramics [34]. In order to utilize the higher electromechanical coupling capability of bulk ceramics,

Aktakka et al. developed a fabrication process to integrate bulk PZT on Si wafers and subsequently thin the ceramic down to obtain a MEMS scale device [34, 45]. Another approach to increase the electromechanical coupling of thin film PZT is using epitaxial growth method [33]. Successful epitaxial growth of PZT thin films on Si substrates using a $SrTiO_3$ buffer layer was demonstrated using pulsed laser deposition [46] and molecular beam epoxy methods [47, 48].

Another widely studied material for MEMS scale PEHs is aluminum nitride (AlN). Despite its significantly lower electromechanical coupling factor, AlN has certain advantages over PZT. First of all, AlN films can be grown sputtering at relatively low temperatures that are safe for CMOS circuits [49]. This is a major advantage over thin film PZT, which requires temperatures exceeding 600 °C for crystallization. Another advantage of AlN is its higher piezoelectric voltage coefficient due to its lower dielectric constant. Although this is simply a trade-off between voltage and current, high voltage provides an important advantage for systems with diode rectifier circuits, where each diode uses some voltage headroom. One of the fundamental differences between AlN and PZT is that the latter is ferroelectric whereas the former is not. AlN thin films have to be deposited under optimized conditions that favor growth along its c-axis in order to exhibit piezoelectricity at macro scale. Consequently, a properly grown AlN thin film does not require any poling treatment. On the other hand, this prevents it from being used with interdigitated electrodes (IDE), which require the material be poled using these electrodes [8]. Marzencki et al. presented theoretical and experimental studies on AlN based MEMS scale PEHs and [50, 51]. They fabricated a system on a package that includes an AlN based PEH and a power management circuit integrated in a single package [51]. Effect of

packaging on the performance of AlN based prototype PEHs was examined by Elfrink et al. [52, 53]. In another study on AlN based MEMS PEHs, Yen et al. proposed a corrugated beam structure in order to increase energy conversion efficiency [54].

In addition to cantilever type devices, MEMS scale pressure mode PEHs were also demonstrated using diaphragm structures coated with thin piezoelectric films. One such example was presented by Horowitz et al., where the authors harvested energy from acoustic waves in air using a sol-gel PZT based diaphragm [55]. Another diaphragm type MEMS scale PEH example, a zinc oxide (ZnO) based device with an optimized electrode pattern, was presented by Kuehne et al. in 2008 [56]. Aside from this example, there are very few MEMS scale PEHs using ZnO [57]. Despite its CMOS compatibility and piezoelectric properties comparable to those of AlN, ZnO is much less preferred in MEMS PEHs due to its low DC resistivity and diffusion problem of Zn ions [58].

1.2.1 Nano-Scale Piezoelectric Energy Harvesters

Piezoelectric energy harvesting at nano scale is typically done using ZnO nanowires. Electrical power generation from ZnO nanowires was first demonstrated by Wang et al. in 2006 [59, 60]. A conductive AFM probe were used to bend the nanowires, which generated voltage spikes rectified by the Schottky contact between the probe and the semiconducting nanowire [59]. After these proof-of-concept studies on single nanowires, the same group developed methods to harvest power from large numbers of nanowires [61, 62]. Utilization of energy harvested from nanowires was also demonstrated in a number of studies [63-65]. These successful demonstrations of nano-scale PEHs attracted a growing interest and led to the founding a dedicated scientific journal, Nano Energy.

1.3 Research Objectives

Among the different size devices discussed in this chapter, MEMS scale PEHs have the highest potential to be integrated into standalone CMOS electronic transducers, since both CMOS and MEMS technologies utilize very similar materials, deposition and photolithographic patterning methods, and industry standard Si wafers. Integrating energy harvesting units with the electronics at chip level would reduce overall dimensions by placing these components in very close proximity, which in turn reduces the unit cost of the devices. System losses due to parasitic impedances are also minimized with this method. Furthermore, microfabricated interconnections are mechanically more reliable compared to bonding wires. However, not all MEMS fabrication techniques are automatically compatible with CMOS. For a monolithic integration to be possible, MEMS process should not include steps that can damage the circuitry such as high temperature annealing or deposition of materials that can diffuse into the circuit area.

The main goal of this thesis work is developing high performance CMOS compatible MEMS scale PEHs that has the potential to be monolithically integrated with CMOS integrated circuits (IC). In order to achieve this goal, proper device architecture, piezoelectric material, and power management circuitry must be chosen; and all these aspects of the work pose certain challenges.

As discussed in the previous subsections, cantilever beam is the most commonly used mechanical structure for vibration energy harvesting. It is possible to utilize cantilever type PEHs in d_{31} or d_{33} modes, the former with piezoelectric material placed between parallel plate electrodes (PPE) and the latter with IDEs deposited on one side of the piezoelectric material. Piezoelectric d_{33} coefficients are higher than d_{31} in all common

piezoelectric materials; therefore, a finite element method (FEM) simulation based study was performed to investigate the feasibility of an IDE based cantilever design in the early steps of this work [66]. One of the interesting results concluded from the results of this FEM study was that despite the higher piezoelectric coefficient, d_{33} mode devices cannot effectively utilize the entire volume of the piezoelectric material for electrical energy generation. This result was corroborated by other comparative studies in the literature [44, 67]. Therefore, subsequent studies were focused on d_{31} mode PEHs.

Selection of the piezoelectric material is probably the most important factor that determines the CMOS compatibility of the PEH. Most commonly preferred material, PZT, is not suitable for CMOS integration due to its high crystallization temperature. CMOS compatible MEMS scale PEHs typically utilize AlN [51-54], although devices with ZnO, another CMOS compatible material, were also reported [57]. Another material class that is much less investigated for PEHs is piezoelectric polymers, most prominently PVDF and its copolymer polyvinylidene fluoride-trifluoroethylene (PVDF-TrFE). Fabrication of PVDF-TrFE microstructures with CMOS compatible MEMS methods have been recently demonstrated [68]. An FEM simulation study was performed by the author in order to compare the performances of these materials for MEMS scale cantilever type PEHs. Obtained results indicated that PVDF-TrFE based devices can outperform AlN based ones in terms of output power [69]. In addition to higher power output, PVDF-TrFE can alleviate the narrow bandwidth problem of cantilever structures due to its low mechanical Q factor. Furthermore, it can accommodate higher strain levels due to its flexible nature as a polymer. Because of these advantages, PVDF-TrFE was selected as the active material. Initially, a proof-of-concept study has been performed to

investigate the energy harvesting capability of PVDF-TrFE at MEMS scale [70]. Performance evaluation of this first generation PEHs was done by bending and releasing the cantilevers with a custom-made probe station setup [70]. After verifying the operation of these proof-of-concept devices, a new set of PEHs that utilize multiple PVDF-TrFE layers were designed and fabricated for improved power output. Second generation PEHs with different dimensions were tested using an electrodynamic mini shaker and results were presented.

Most systems require a DC voltage to operate; therefore, converting the AC voltage generated by PEHs to DC and transferring to an energy storage unit is also an important part of energy harvesting systems. The efficiency of this energy transfer operation becomes more critical at smaller scales since the available power is already low. In addition, forward voltage drops of diodes, which are commonly used for AC-DC conversion, pose a significant challenge for MEMS scale devices due to low output voltage values. In order to improve the harvester efficiency and increase the output voltage magnitude, synchronized switch harvesting on inductor (SSHI) methods were studied. SSHI method utilizes an inductor connected to the PEH through a switch, which is turned on very briefly at the voltage peaks to invert the voltage polarity [71, 72]. The switch/inductor interface can be connected in parallel or in series with the PEH without significantly affecting the overall efficiency [73, 74]. However, parallel implementation is significantly advantageous for MEMS scale PEHs since it does not require the open circuit PEH voltage to exceed diode turn on voltages for rectification [74]. A parallel-SSHI circuit was designed at both transistor level and board level. Transistor level circuit was designed using NCSU CDK v1.6.0.beta, a free design kit based on a 0.6 μm CMOS

process, and circuit operation was verified by simulations. Same circuit topology was adapted to discrete components for a board-level design. A printed circuit board (PCB) was designed, fabricated, and characterized in detail. Fabricated PCBs were also integrated with second generation PEHs for system level performance evaluation.

1.4 Thesis Organization

Chapter 2 discusses the theory of piezoelectric energy harvesting. A general definition of the piezoelectricity is given. Direct piezoelectric effect is discussed and the formula for electromechanical coupling factor is derived by using piezoelectric constitutive equations on a simple piezoelectric energy harvester model. Then, the mechanics of cantilever beams, which are the most commonly used structures in piezoelectric energy harvesters, are discussed. Important formulae for unimorph piezoelectric cantilevers are also derived using linear beam theory.

Chapter 3 presents the studies performed to determine the architecture and piezoelectric material for the proposed CMOS compatible energy harvester. In the first section of this chapter, the results of an FEM study on the electrode pattern optimization are summarized. The next section discusses the advantage and disadvantages of CMOS compatible piezoelectric materials and presents the results of an FEM study comparing their energy harvesting potentials. The final section of Chapter 3 discusses the three structural layer options for MEMS scale piezoelectric energy harvesters.

Chapter 4 presents a comprehensive characterization of the fabricated PVDF-TrFE films, including the dielectric, ferroelectric, and piezoelectric properties.

Chapter 5 presents the encountered problems and developed solutions during PVDF-TrFE thin film fabrication. Design methodology and fabrication process steps used for

the two device generations in this study, single-layer proof-of-concept PEHs and optimized multi-layer PEHs, are described in detail. The results of electromechanical energy conversion tests of the fabricated prototypes are given.

Chapter 6 presents the studies on the integration of the fabricated PEHs with external electronics for improved energy harvesting performance. Theoretical basis of parallel SSHI is discussed after a brief introduction to power conditioning circuits for PEHs. Both transistor and board level designs are presented along with their respective theoretical analyses, simulations, and experimental results. Energy harvesting performance of the integrated system, consisting of the PEH and SSHI circuit, was evaluated and compared to the standalone operation of the PEH.

Finally, Chapter 7 gives a summary of the work presented in this dissertation, draws conclusions, and gives an outline of the future work envisioned for the further development of the CMOS compatible PEH concept using piezoelectric polymers.

CHAPTER 2: PIEZOELECTRIC ENERGY HARVESTING THEORY

Piezoelectric devices can be used to harvest energy from various sources such as mechanical impacts, varying pressure fields, and vibrations. Depending on the type of the energy source, PEHs are designed with different mechanical architectures such as stacks, cantilevers, or membranes. Despite the different architectures, all PEHs share the same basic energy conversion mechanism, which is the direct piezoelectric effect. Therefore, a thorough understanding of the direct piezoelectric effect is crucial for the design and modeling of PEHs. This chapter first describes the piezoelectricity and the constitutive equations that govern the relationship between the mechanical and electrical domains in piezoelectric materials. Then, basic theoretical calculations on piezoelectric energy harvesting are presented using the constitutive equations. Finally, the mechanics of cantilever type PEHs, which are the most widely preferred devices for vibration energy harvesting, are discussed and equivalent models are presented.

2.1 Piezoelectricity Phenomenon

The word piezoelectricity defines the phenomenon of electromechanical energy conversion observed in piezoelectric materials, which generate an electrical charge in response to mechanical stress (direct piezoelectric effect) or reciprocally, generate mechanical strain in response to an applied electric field (inverse piezoelectric effect). Electrical or mechanical output generated by the piezoelectric material is proportional to the amplitude of the applied input. The linear equations that govern the piezoelectric effect, named piezoelectric constitutive equations, can be shown in matrix notation as

$$\begin{bmatrix} S \\ D \end{bmatrix} = \begin{bmatrix} s^E & d \\ d & \varepsilon^T \end{bmatrix} \cdot \begin{bmatrix} T \\ E \end{bmatrix} \tag{2.1}$$

where S is the strain, D is the electric displacement, s is the elastic compliance, d is the piezoelectric charge coefficients for strain-charge form, ε is the dielectric permittivity, T is the stress, and E is the electric field. The superscripts E and S indicate the coefficients measured at constant electric field and constant strain, respectively [75]. Piezoelectric energy harvesting makes use of the direct piezoelectric effect, which is governed by the second row of Equation (2.1). The expanded and simplified form of this equation is

$$\begin{bmatrix} D_1 \\ D_2 \\ D_3 \end{bmatrix} = \begin{bmatrix} d_{11} & d_{12} & d_{13} & d_{14} & d_{15} & d_{16} \\ d_{21} & d_{22} & d_{23} & d_{24} & d_{25} & d_{26} \\ d_{31} & d_{32} & d_{33} & d_{34} & d_{35} & d_{36} \end{bmatrix} \begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \end{bmatrix} + \begin{bmatrix} \varepsilon_{11} & \varepsilon_{12} & \varepsilon_{13} \\ \varepsilon_{21} & \varepsilon_{22} & \varepsilon_{23} \\ \varepsilon_{31} & \varepsilon_{32} & \varepsilon_{32} \end{bmatrix} \begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} \tag{2.2}$$

where the subscript indices denote different directions. The convention for most piezoelectric materials is to assign index 3 to the axis along which the polarization occurs. Indices 1 and 2 denote the other two mutually orthogonal coordinate axes, forming a Cartesian coordinate system. Indices from 4 to 6 are present only in stress and strain vectors, and they denote the rotational stress and strains along the axes from 1 to 3, respectively.

In order for piezoelectricity to be observed at a macroscopic scale, the effects from individual crystalline regions should not cancel each other. This requirement is readily satisfied in single crystal materials; however, most piezoelectric materials are not single crystals. In case of polycrystalline materials, induction of piezoelectric behavior at macro scale can be achieved via different methods depending on the ferroelectricity of the material. Piezoelectric films of non-ferroelectric materials such as AlN and ZnO can be obtained by optimizing the deposition process to form highly oriented films that grow along their c-axis [58]. Consequently, a properly deposited AlN or ZnO film exhibits

piezoelectricity without any further treatment. On the other hand, ferroelectric materials have a spontaneous polarization due to the non-zero dipole moments in their unit crystal cells, and the direction of this polarization can be modified by an external electric field. This eliminates the need to grow a highly oriented film; polarization directions of crystalline regions in a ferroelectric material can be aligned by applying a strong electric field. The process of aligning the polarization directions in a ferroelectric material is called poling, which is illustrated in Figure 2.1. The remnant polarization in the material after the voltage is removed causes a hysteresis in the voltage-polarization curve, which is a distinguishing characteristic of ferroelectric materials.

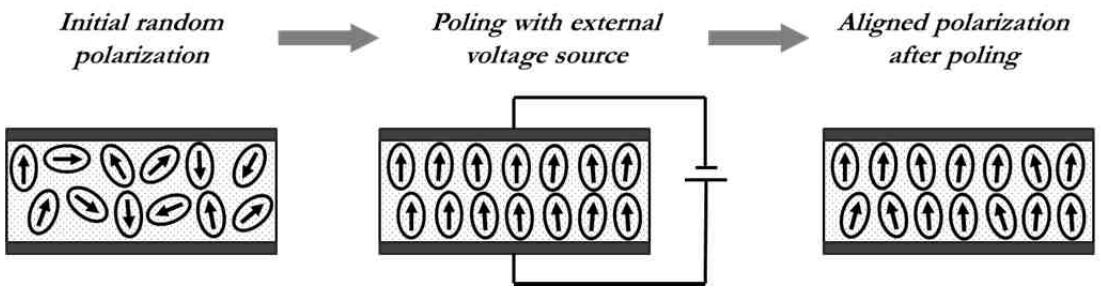


Figure 2.1: Illustration of the poling process. Randomly oriented crystalline domains are aligned by an external voltage, and the alignment is preserved after the voltage is removed.

2.2 Energy Harvesting Using Direct Piezoelectric Effect

Piezoelectric energy harvesting is based on the principle of utilizing the direct piezoelectric effect in order to convert mechanical energy into electrical energy. As indicated by Equation 2.2, there is a linear relationship between the electrical displacement and mechanical stress, and the slope is determined by the corresponding piezoelectric coefficients. Although piezoelectric coefficient matrix d consists of 18 coefficients, the number of independent coefficients is usually less, depending on the

crystal class of the material [75]. For example, poled PZT ceramics, which have a perovskite crystal structure, have 3 independent non-zero piezoelectric coefficients, d_{31}, d_{33}, and d_{15} [76]. On the other hand, PVDF-TrFE has an orthorhombic crystal structure and it has 5 independent non-zero piezoelectric coefficients [77]. Piezoelectric matrix structures for these two materials are shown in Figure 2.2. For both materials, shear strain related coefficients, d_{15} and d_{24}, are the highest, followed by d_{33}, and the lowest are d_{31} and d_{32} [77, 78]. Despite the high coefficient, shear mode is not preferred in energy harvesting since inducing shear stress is not as easy as normal stress. The next highest coefficient, d_{33}, is easier to utilize, and therefore, it has been widely studied in the literature.

PZT

$$\begin{bmatrix} 0 & 0 & 0 & 0 & d_{15} & 0 \\ 0 & 0 & 0 & d_{15} & 0 & 0 \\ d_{31} & d_{31} & d_{33} & 0 & 0 & 0 \end{bmatrix}$$

PVDF-TrFE

$$\begin{bmatrix} 0 & 0 & 0 & 0 & d_{15} & 0 \\ 0 & 0 & 0 & d_{24} & 0 & 0 \\ d_{31} & d_{32} & d_{33} & 0 & 0 & 0 \end{bmatrix}$$

Figure 2.2: Piezoelectric coefficient matrix structures for PZT and PVDF-TrFE. Although both materials have 5 non-zero coefficients, only 3 of these are independent in PZT.

The most straightforward method to harvest energy in d_{33} mode is simply using a piezoelectric block with electrodes on its surfaces perpendicular to the poling axis and applying stress to these surfaces, which is illustrated in Figure 2.3 with a simplified drawing. In this case, the capacitance of the PEH, charge and voltage generated in this capacitor, and corresponding electrical energy are equal to

$$C_{piezo} = \frac{\varepsilon_3 \cdot w \cdot l}{t} = \frac{\varepsilon_3 \cdot A}{t} \tag{2.3}$$

$$Q_{piezo} = \oiint D_3 \cdot dA = D_3 \cdot A = d_{33} \cdot T \cdot A \tag{2.4}$$

$$V_{piezo} = \frac{Q_{piezo}}{C_{piezo}} = \frac{d_{33} \cdot T \cdot t}{\varepsilon_3} \tag{2.5}$$

$$\mathrm{W}_e = \frac{1}{2} \cdot Q \cdot V = \frac{{d_{33}}^2 \cdot T^2 \cdot t \cdot A}{2\varepsilon_3} \tag{2.6}$$

where w, l, and t are the dimensions of the piezoelectric element as shown on the figure, and d_{33} and ε_3 are the piezoelectric and dielectric coefficients along the polarization axis, respectively. On the other hand, the mechanical energy stored in the same piezoelectric block is equal to

$$\mathrm{W}_m = \frac{1}{2} \cdot T \cdot S = \frac{s_{33} \cdot T^2 \cdot t \cdot A}{2} \tag{2.7}$$

where s_{33} is the compliance coefficient along the polarization axis.

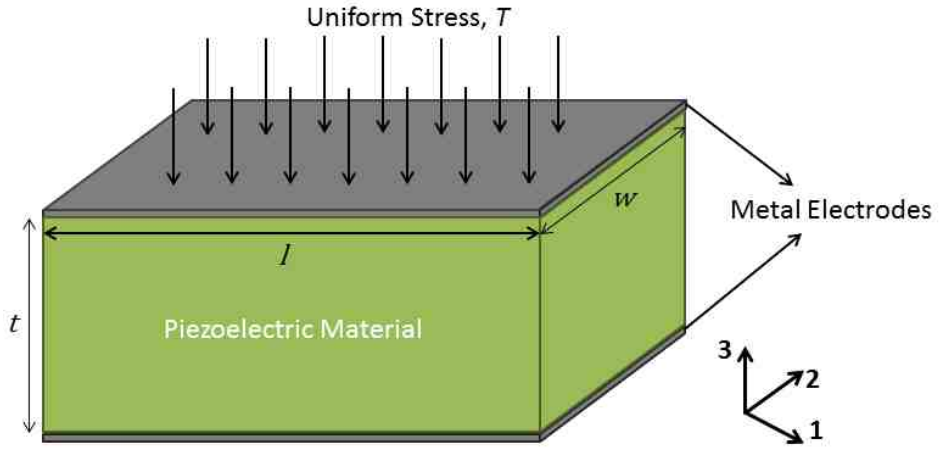


Figure 2.3: A simple d_{33} mode PEH consisting of a metallized piezoelectric material block with a thickness t and a surface area of $A = l \times w$.

The ratio of the electrical output energy to the mechanical input energy is defined as the electromechanical coupling factor, which can be calculated from Equations 2.6 and 2.7 as

$$k_{33}{}^2 = \frac{\mathrm{W}_e}{\mathrm{W}_m} = \frac{d_{33}{}^2}{s_{33} \cdot \varepsilon_3} \tag{2.8}$$

As indicated by Equation 2.8, electromechanical coupling factor is a function of material properties. Nevertheless, overall performance of the PEHs does not depend only on the electromechanical coupling factor; it is also proportional to the mechanical energy stored in the piezoelectric material as well as its volume. Therefore, the simple PEH illustrated in Figure 2.3 is not a very efficient structure; most materials have a high bulk modulus, which results in small strains and hence small mechanical energy. To exemplify, electrical energy density in a 200 μm-thick PZT-5H block subjected to a uniform pressure of 1 atm would be approximately equal to 1.2 nJ/cm^2. The reason for this low energy density despite the high electromechanical coupling factor is the small strain; 1 atm uniform pressure can only create a strain of 2.1×10^{-6}, which corresponds to a mechanical energy of approximately 2.1 nJ/cm^2. Therefore, PEHs frequently utilize mechanical structures that create large strains from a given mechanical force, such as cantilevers or thin membranes. The main trade-off of using these structures is the reduced piezoelectric material volume, which has a positive correlation with the total electrical energy generated by the device. Another approach is to keep the bulk piezoelectric and increase the stress using mechanical force amplifiers such as hydraulic amplifiers or cymbal structures [13, 29-31]. However, this second approach is obviously not suitable for MEMS scale PEHs due to fabrication limitations; therefore, MEMS scale PEHs always use mechanical structures with high mechanical compliances.

2.3 Cantilever Type Piezoelectric Energy Harvesters

Cantilever beams are the most widely used mechanical structures in PEHs for a number of reasons, including the high average strain generated per unit force, low resonance frequency, and simple structure [6]. Figure 2.4 shows a bent cantilever beam and the resultant strains along its thickness. As illustrated in the figure, bottom surface of the cantilever elongates while the top surface shortens when the cantilever bends upward, creating both tensile and compressive stresses on the beam. The surface with zero strain at the boundary of the compressive and tensile strains is called the neutral axis.

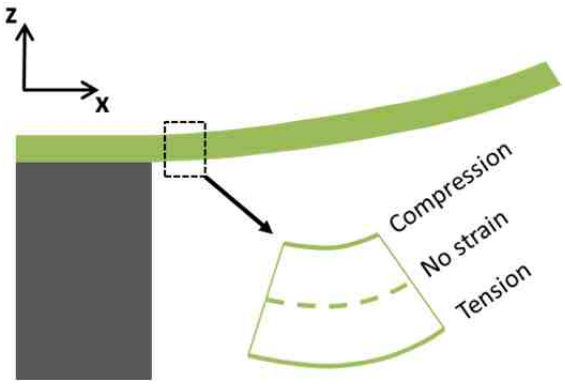


Figure 2.4: Bent cantilever beam and cross-sectional view showing the resultant stresses. The hypothetical plane with zero strain, shown with dashed line, is called the neutral axis.

An efficient cantilever type PEH design is a bimorph, where piezoelectric materials are placed on both sides of a central structural layer in order to harvest energy from both compressive and tensile stresses. The geometrically symmetric design of a bimorph ensures that the neutral axis stays inside the central non-piezoelectric layer; therefore, the strain sign is the same within each piezoelectric layer. Bimorph cantilever is the preferred mechanical architecture in most meso-scale vibrational PEHs due to its high overall electromechanical conversion efficiency [6, 18, 19]. However, creating bimorph

cantilevers is very difficult, if not impossible, using MEMS fabrication techniques [33]. Therefore, cantilever type PEHs are fabricated in unimorph configuration in MEMS scale.

2.3.1 Theoretical Analysis of a Bent Cantilever Beam

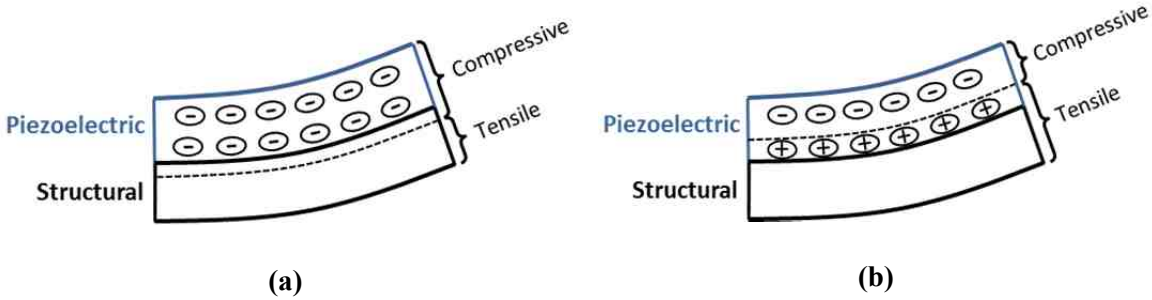
Unimorph cantilevers have a single piezoelectric layer deposited on a structural layer, which provides mechanical sturdiness since most piezoelectric materials are brittle. Another important function of the structural layer in a unimorph cantilever is to keep the neutral axis outside the piezoelectric material, which prevents charge cancellation due to opposite strain signs. Position dependent strain in a thin cantilever beam for small deformations can be calculated using the well-established Euler-Bernoulli beam theory. According to this model, the longitudinal strain in a bent cantilever beam depends on the curvature of the beam as well as location along beam thickness, and it is equal to

$$S(x,z) = \mathbb{C}(x) \cdot (z - z_n) \tag{2.9}$$

where $\mathbb{C}$ is the curvature of the beam and z_n is the location of the neutral axis [79]. As evident from this equation, longitudinal stress changes sign along the neutral axis. Figure 2.5 (a) shows the cross section of a unimorph PEH with a properly designed neutral axis location. In this design, the entire piezoelectric layer is under compressive stress, which means that generated electric fields are in the same direction. If the neutral axis is located inside the piezoelectric layer as illustrated in Figure 2.5 (b), electric fields in opposite directions generated by compressive and tensile stress regions will cancel each other and reduce the net electrical output. The location of the neutral axis in a multi-layer cantilever depends on the elastic properties and thicknesses of the layers, and it can be calculated by solving the equation

$$\int_t c_i(z - z_n)dz = 0 \tag{2.10}$$

where c_i is the effective elastic modulus of each layer, z_n is the z-coordinate of the neutral axis, and the integral is taken over the entire thickness t of the beam [80].



(a) **(b)**

Figure 2.5: (a) Neutral axis is located inside the structural layer; the piezoelectric layer is completely under compressive stress. (b) Neutral axis is located inside the piezoelectric layer, where opposite-sign strains cause charge cancellation.

Cantilever beams can be modeled as linear spring-mass systems for small displacements. The equivalent spring constant can be calculated by deriving a formula that relates a force applied at the tip to the corresponding displacement. Figure 2.6 shows a simplified drawing of a thin cantilever beam of length L bent under a point force F applied to its tip.

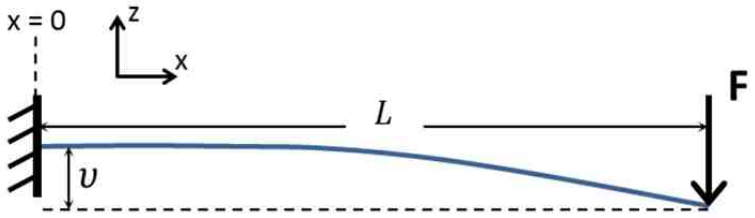


Figure 2.6: A thin cantilever beam of length *L* bent under a point force *F* applied to its tip.

The moment at any point along the length of the beam in Figure 2.6 is equal to

$$M(x) = c \cdot I \cdot \mathbb{C} = F \cdot (L - x) \tag{2.11}$$

where c is the longitudinal elastic modulus and I is the moment of inertia [79]. For small displacements, curvature of the beam can be approximated as

$$\mathbb{C} = \frac{d^2 v}{dx^2} \tag{2.12}$$

where v is the z-displacement. Placing Equation (2.12) into (2.11) and integrating it twice with respect to variable x results in the following equation

$$v(x) = \frac{F}{cI} \cdot \left(\frac{Lx^2}{2} - \frac{x^3}{6} + Ax + B \right) \tag{2.13}$$

where A and B are constants that need to be evaluated by applying the boundary conditions $v = 0$ and $dv/dx = 0$. The displacement of the curve along the z-axis is then found as

$$v(x) = \frac{F}{cI} \cdot \frac{x^2}{2} \cdot \left(L - \frac{x}{3} \right) \tag{2.14}$$

The tip displacement and corresponding spring constant of the cantilever can then be written as

$$v_{tip} = \frac{F}{cI} \cdot \frac{L^3}{3} \tag{2.15}$$

$$\mathrm{K}_{eqv} = \frac{3 \cdot cI}{L^3} \tag{2.16}$$

It should be noted that this spring constant is calculated using linear approximations, which are valid for tip displacements up to approximately 15% of the cantilever length [81].

In case of a uniform, single-layer cantilever, moment of inertia is equal to

$$I = \frac{wt^3}{12} \tag{2.17}$$

where *w* and *t* are the width and thickness of the cantilever, respectively. For cantilevers with multiple layers of different materials, evaluation of the integral for the moment of inertia for each layer yields

$$I_{ml} = \int_w \int_t (z - z_n)^2 dz \cdot dy = \sum_i \left[\frac{w_i {t_i}^3}{12} + w_i t_i \left(z_{m,i} - z_n \right)^2 \right] \tag{2.18}$$

where subscript *i* indicates different layers, and z_m is the *z*-coordinate of the midpoint of each layer. Using equations (2.16) and (2.18), equivalent spring constant of a multi-layer cantilever can be written as

$$K_{eqv,ml} = \frac{3}{L^3} \cdot \sum_i \left\{ c_i \cdot \left[\frac{w_i {t_i}^3}{12} + w_i t_i \left(z_{m,i} - z_n \right)^2 \right] \right\} \tag{2.19}$$

The resonance frequency of the cantilever can then be calculated from this equivalent spring constant and equivalent mass referred to the cantilever tip. The equivalent mass due to the beam itself is equal to

$$m_{tip} = \frac{33}{140} \cdot m_{cantilever} \tag{2.20}$$

where $m_{cantilever}$ is the total mass of the cantilever [82]. However, the equivalent mass is usually dominated by the proof mass in PEHs. Since the proof mass is usually placed as close as possible to the cantilever tip, its mass, m_{PM}, can be directly added to the equivalent tip mass. Then, the undamped resonance frequency of the beam can be calculated in Hz using the formula

$$f_n = \frac{1}{2\pi} \cdot \sqrt{\frac{K_{eqv}}{m_{eqv}}} = \frac{1}{2\pi} \cdot \sqrt{\frac{K_{eqv}}{m_{tip} + m_{PM}}} \tag{2.21}$$

A more accurate resonance frequency calculation requires the damping be taken into consideration as well since the damped frequency is equal to

$$f_n^d = f_n\sqrt{(1-\xi^2)} \tag{2.22}$$

where ξ is the damping ratio. However, unlike the spring constant and the mass, damping parameters arise from different sources depending on the device, including the internal mechanical losses inside the cantilever, air damping, and damping due to electrical load. As a result, damping parameters of PEHs are much more difficult to express using analytical formulae. Damping ratio also determines the mechanical Q factor of the cantilever; a lower damping corresponds to higher peak displacement at resonance, increasing the Q.

As discussed in Section 2.2, generated electrical energy is proportional to the total mechanical energy stored in the piezoelectric material. Curvature of the beam can be expressed in terms of the tip displacement by placing Equation (2.15) into (2.11)

$$\mathbb{C}(x) = 3v_{tip}\frac{L-x}{L^3} \tag{2.23}$$

Placing this equation into Equation (2.9) gives the formula for position dependent strain as

$$S(x,z) = 3v_{tip}\frac{L-x}{L^3}(z-z_n) \tag{2.24}$$

This equation shows that strain is maximum at the base and decreases towards the tip of the cantilever, reaching 0 at $x = L$. Therefore, cantilever type PEHs usually utilize electrodes that cover only a portion of the cantilever length. Integrating equation (2.24) over the piezoelectric material volume from $x = 0$ to $x = L_e$ yields

$$S_{piezo,int}(L_e) = 3\frac{v_{tip}}{L^2}wL_e\left(1-\frac{L_e}{2L}\right)t_p\left(z_{m,p}-z_n\right) \tag{2.25}$$

where t_p and $z_{m,p}$ are the thickness and mid-point z-coordinate of the piezoelectric layer, respectively. Average strain in the same piezoelectric material region can be calculated as

$$S_{piezo,avg}(L_e) = 3\frac{v_{tip}}{L^2}\left(1 - \frac{L_e}{2L}\right)\left(z_{m,p} - z_n\right) \tag{2.26}$$

by simply dividing the integrated stress by the material volume.

The bending strain along the cantilever length might cause stress or strain along other axes due to Poisson's effect. If the film was completely free to move along film thickness (z-axis) or cantilever width (y-axis), there would be zero stress along these two axes. This is a reasonable approximation for z-axis in case of a cantilever with a thin film piezoelectric, since the top surface of the film is not constrained. On the other hand, structural layers can restrict the movement of piezoelectric layer along y-axis, which would limit the strain and cause non-zero stress along this axis. The stress values along x and y axes can be calculated for two extreme cases, one with no clamping effect (zero stress along y) and the other with full clamping (zero strain along y), using the constitutive equations. These two extreme cases then can be used to determine a range for the expected piezoelectric output. If the indices 1, 2, and 3 in the constitutive equations are assigned x, y, and z axes respectively, the stress along film thickness can be written as

$$T_3 = c_{31}S_1 + c_{32}S_2 + c_{33}S_3 = 0 \tag{2.27}$$

where c_{ij} are the coefficients of the stiffness matrix. The strain along the z-axis is then equal to

$$S_3 = -\left(\frac{c_{31}}{c_{33}}S_1 + \frac{c_{32}}{c_{33}}S_2\right) \tag{2.28}$$

In case of a film unrestricted along cantilever thickness, the stress along y-axis, T_2, should be zero. Then the strain along the same axis becomes equal to

$$S_2 = -\left(\frac{c_{21}}{c_{22}}S_1 + \frac{c_{23}}{c_{22}}S_3\right) \tag{2.29}$$

Solving equations (2.28) and (2.29) together gives the strains along *y* and *z* axes in terms of the bending strain as

$$S_2 = -\frac{c_{21}c_{33} - c_{23}c_{31}}{c_{22}c_{33} - c_{32}c_{23}} \cdot S_1 \tag{2.30}$$

$$S_3 = -\frac{c_{31}c_{22} - c_{32}c_{21}}{c_{22}c_{33} - c_{32}c_{23}} \cdot S_1 \tag{2.31}$$

Using these equations, the stress along the *x* axis can be written as

$$T_{1,free} = \left(c_{11} - c_{12}\frac{c_{21}c_{33} - c_{23}c_{31}}{c_{22}c_{33} - c_{32}c_{23}} - c_{13}\frac{c_{31}c_{22} - c_{32}c_{21}}{c_{22}c_{33} - c_{32}c_{23}}\right) \cdot S_1 \tag{2.32}$$

in terms of the bending strain.

The same analysis can be done for a piezoelectric film with zero strain along cantilever width due to clamping by structural layers. In this case, equation (2.28) becomes

$$S_3 = -\frac{c_{31}}{c_{33}} S_1 \tag{2.33}$$

which results in an x-axis stress of

$$T_{1,clamped} = \left(c_{11} - c_{13}\frac{c_{31}}{c_{33}}\right) \cdot S_1 \tag{2.34}$$

Unlike the free thin film case where only stress component is along the *x*-axis, there would be a non-zero stress along the *y*-axis due to substrate clamping. The magnitude of this stress can be written in terms of the bending strain as

$$T_{2,clamped} = c_{21}S_1 + c_{23}S_3 = \left(c_{21} - c_{23}\frac{c_{13}}{c_{33}}\right) \cdot S_1 \tag{2.35}$$

It should be noted that this stress would also contribute to the piezoelectric output via d_{32} coefficient. Therefore, the output is expected to be higher if the piezoelectric material is clamped by the substrate. On the other hand, zero strain case is mostly only hypothetical;

even if the structural layers are stiff enough to completely clamp the piezoelectric material, they would have non-zero strains along *y*-axis due to Poisson's effect. Nevertheless, it can be used to determine an upper bound for the electrical output of a cantilever type PEH.

2.3.2 Equivalent Circuit Models for Cantilever Type PEHs

PEHs aim to generate electrical energy for immediate or later use; therefore, the electric field generated inside the piezoelectric material needs to be converted into voltage and transferred to some electrical circuitry. This task can be done by electrodes placed in the close vicinity of the piezoelectric material. An electric field between two electrodes creates a voltage that can be calculated using the contour integral

$$V = \oint \vec{E} \cdot d\vec{l} \tag{2.36}$$

which can be taken along any path. Depending on the configuration of these electrodes, it is possible to use different piezoelectric modes in cantilever type PEHs. Figure 2.7 shows a simplified diagram of two common electrode configurations.

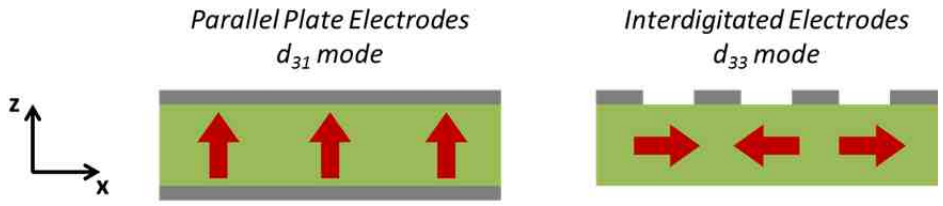


Figure 2.7: Parallel plate and interdigitated electrode configurations for cantilever type PEHs. Red arrows show the polarization direction inside the piezoelectric materials. Cantilever length and thickness are along x and z axes, respectively.

The dominant strain in a bent cantilever is always longitudinal, i.e. along *x*-axis as shown in Figure 2.4. However, polarization axis of the piezoelectric material can be

different. For most piezoelectric materials, only non-zero coefficients for normal strains are d_{31}, d_{32}, and d_{33}, all of which generate electric polarization along axis 3. Therefore, the electrodes must be along axis 3, i.e., polarization axis, to be able to harvest the electrical energy. This requirement limits the electrode placement options in non-ferroelectric materials such as AlN and ZnO since these piezoelectric films are grown with a c-axis orientation along thickness, which cannot be changed later. Therefore, the electrodes have to be placed at the top and the bottom of these films. The same electrode placement can be used in ferroelectric materials as well. In this PPE architecture, axis 3 is along the cantilever thickness whereas the strain is along cantilever length. Consequently, electric displacement is related to stress via piezoelectric coefficient d_{31}, and therefore, the PEH is said to operate in d_{31} mode. The other approach, using IDEs, is only applicable to ferroelectric materials since this method requires the material be poled using the same electrodes. In this method, IDEs are deposited on one side of the material and used to pole it along the cantilever length. As a result, the polarization and the strain are on the same axis, and the device operates in d_{33} mode.

The electrode configuration has a profound effect on the electrical parameters of the device. PPEs form a simple capacitor with a well-defined area and dielectric thickness; therefore, the capacitance can be easily calculated using Equation (2.3). MEMS scale PEHs usually have thin film piezoelectric materials, which limits the electrode distance to micrometer range, while electrode areas can be made much larger. As a result, PPE type devices typically have large capacitance; however, their voltage amplitude is limited due to limited distance between the electrodes as indicated by Equation (2.26). On the other hand, exact capacitance calculation of an IDE involves complicated steps such as elliptic

integrals [83]. Although easier methods for approximate calculations are also available [84], these methods assume a uniform dielectric constant. However, polarization pattern of the piezoelectric material depends on the IDE geometry, and it is quite complicated especially at MEMS scale [66, 85-87]. Nevertheless, uniform poling assumptions are acceptable if the electrode spacing is much smaller than the finger length, and at least comparable with finger width [66]. In general, capacitance of an IDE covering a constant area is inversely proportional to finger distance, whereas the output voltage increases with increasing finger distance. This trade-off between the capacitance and voltage can be adjusted by simply changing the electrode pattern, which provides a much greater flexibility compared to PPE devices [37].

The basic structure of PEHs, metal electrodes on a dielectric material, is basically a non-ideal capacitor with dielectric losses and leakage. In the presence of a varying mechanical strain, the piezoelectric material generates a proportional charge density at the electrode surfaces, which is equivalent to driving this capacitor with a current source [88]. However, PEHs usually require more comprehensive models that include the frequency response of the structure. Different equivalent circuit models (ECM) developed for this purpose can be found in the literature [6, 89, 90]. Figure 2.8 shows a comprehensive ECM for PEHs, where mechanical and electrical domains modeled with passive circuit elements and coupled via dependent sources [6, 90]. In the mechanical side, passive components L_m, R_d, and C_k represent the inertia, mechanical damping, and stiffness of the cantilever, respectively. The electrical domain simply consists of the piezoelectric capacitor with capacitance C_p and its leakage resistance R_L. The quantities analogous to voltage and current at the mechanical side are stress and time derivative of

strain, respectively [6]. Electromechanical energy conversion is modeled with two dependent sources, a voltage dependent voltage source at the mechanical side, and a current dependent current source at the electrical side. The conversion factors of these dependent sources, α and β, are proportional to the electromechanical coupling strength. The circuit can be simplified by reflecting the impedance at the electrical side to the mechanical side as also shown in Figure 2.8. The reflection ratio is the product of the two conversion factors, yielding a reflected impedance of $\alpha \cdot \beta \cdot Z_L$, where Z_L is the total impedance at the electrical side. This result implies that the effect of the electrical load on the mechanical response depends on electromechanical coupling strength.

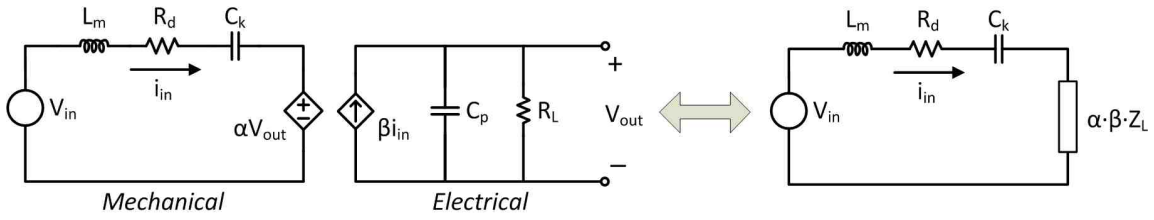


Figure 2.8: A comprehensive ECM for PEHs [90]. In the mechanical domain, V_{in}, L_m, C_k, and R_d represent the input stress, inertia, compliance, and damping, respectively. Electrical domain consists of only the piezoelectric capacitor and its leakage resistance. Coupling between the domains is modeled with the dependent sources. Electrical domain impedance can be reflected on the mechanical side by multiplying it with ($\alpha \cdot \beta$).

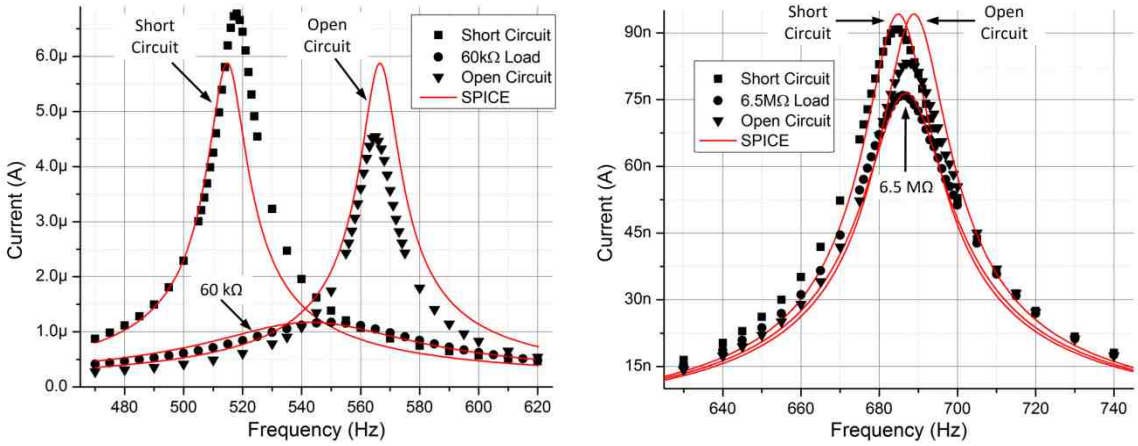
ECMs provide a convenient way to model the behavior of PEHs integrated with external circuitry. In addition, the effect of various parameters on the PEH performance can be examined very quickly using standard circuit simulation tools. On the other hand, most of these models use a number of assumptions while calculating the parameters. Furthermore, using lumped elements to model the devices can leave out the localized effects such as fringing fields around electrode edges or other non-idealities. Nevertheless, these effects are not usually significant, especially at meso-scale and larger

cantilevers, as also verified by experiments [6]. In order to examine the accuracy of the same model at MEMS scale, a comparative study was performed using FEM simulations run in COMSOL Multiphysics. Figure 2.9 shows the 2D FEM and SPICE simulation results for the output currents of MEMS scale PEHs that utilize (a) PZT-5H and (b) AlN as the piezoelectric layer. Both PEH models were designed to have a (1000 μm × 1000 μm × 2 μm) Si_3N_4 structural layer and a (200 μm × 1000 μm × 500 μm) Si proof mass at the tip. Piezoelectric layer thickness was chosen as 2.0 μm for PZT; however, it was reduced to 1.5 μm for AlN in order to ensure that the neutral axis stays inside the Si_3N_4 layer. 2D simulations were run with plane strain approximation option, which assumes that the strain along the third dimension is zero. Therefore, the same assumption was used to calculate the ECM parameters, and equivalent stiffness parameters were calculated using equations (2.34) and (2.35). Obtained results show a very good match between SPICE and COMSOL simulations except for the current amplitude of the PZT-based devices under short-circuit and open-circuit conditions, where the discrepancy was found to be as high as 25%. Nevertheless, considering the much smaller time and memory requirements of SPICE simulations, it can be concluded that using ECMs is more feasible to study the effects of various parameters on the device performance. More detailed FEM analyses run on 3D models can then be used for the fine tuning of the designs.

The effect of electrical load on the mechanical response of PEHs can also be observed in Figure 2.9. Overall electromechanical coupling coefficient of a resonant piezoelectric structure can be calculated using the formula

$$k_{PEH} = \frac{\omega_{oc}^2 - \omega_{sc}^2}{\omega_{oc}^2} \tag{2.37}$$

where ω_{oc} and ω_{sc} denote the open-circuit and short-circuit resonance frequencies [91]. Using this equation, the electromechanical coupling factors of the modeled PZT-5H and AlN based devices can be calculated as 15.9% and 0.87%, respectively.



(a) **(b)**

Figure 2.9: Comparison of 2D FEM and SPICE simulations for MEMS scale PEHs that utilize (a) PZT and (b) AlN as the piezoelectric layer. Results show a very good match between the results of the two methods except for the open-circuit and short-circuit current amplitudes of PZT.

An important consequence of the effect of electrical loading on the mechanical response is the change in the resultant output current. When connected to an optimal resistive load of 60 kΩ, the peak output current of the PZT-5H based device drops from 5.9 μA to 1.2 μA according to the ECM simulations, corresponding to an 80% reduction. On the other hand, the reduction for the same condition is only 19% for AlN based device. This is due to the much smaller electromechanical coupling factor of the latter. As shown in Figure 2.8, the value of electrical impedance Z_L is equal to $\alpha \cdot \beta \cdot Z_L$ when reflected to the mechanical side. In case of weakly coupled systems, where the product $\alpha \cdot \beta$ is

small, overall impedance at the mechanical side is not significantly affected by the electrical impedance. This phenomenon can be intuitively explained by the energy removed from the harvester in each motion cycle. A higher percentage of the mechanical energy is removed from the system by the electrical load in case of strongly coupled systems, reducing the vibration amplitude. As a matter of fact, this aspect of piezoelectric materials with high coupling factors has been used for structural vibration damping [91]. In case of weakly coupled systems, vibration amplitude, and consequently the PEH current, are relatively independent from the electrical load. Figure 2.10 shows a simplified model that can be used for these weakly coupled systems, where the mechanical side and transformer of the comprehensive ECM are replaced with an AC current source.

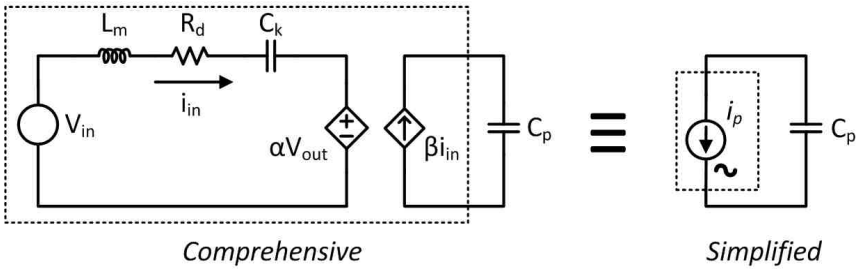


Figure 2.10: Simplified model for PEHs with weak electromagnetic coupling. Due to limited effect of the electrical load on mechanical response, AC current amplitude depends only on the mechanical input.

The simplified model presented in Figure 2.10 was used to model the PEHs during the course of this study, since PVDF-TrFE also has a low electromechanical coupling factor compared to PZT.

CHAPTER 3: STUDIES ON ARCHITECTURE AND PIEZOELECTRIC MATERIAL

Piezoelectric energy harvesting from vibrations can be done using different mechanical structures, device operation modes, and piezoelectric materials. The advantage and disadvantages of each option need to be considered and examined in order to determine the optimal choice for the targeted energy source, application, and device dimensions. Suspended structures, specifically cantilever beams, are widely used in MEMS scale PEHs for their high strain/force ratio attainable by bending. Therefore, cantilever beam is selected as the mechanical structure for the targeted CMOS compatible MEMS scale PEHs. The choices for the electrode architecture, piezoelectric material, and structural layers for these cantilever type PEHs are discussed in this chapter.

The next section presents the results of the FEM studies on the optimization the IDE architecture, which was initially considered due to the higher piezoelectric coefficient d_{33} utilized by IDEs. However, the results of these FEM studies suggested that the utilization efficiency of the mechanical strain drops as the piezoelectric material thickness increases due to the unilateral electrode placement. As a result, subsequent studies were focused on PPE architecture, where the electrical output from the entire piezoelectric material between the electrodes can be utilized. In Section 3.2, potential piezoelectric materials are discussed, and the results of FEM simulations comparing the performances of the CMOS compatible materials AlN, ZnO, and PVDF-TrFE are presented. PVDF-TrFE came out as the material of choice due to its higher power output potential along with a number of other advantages. Finally, three possible alternatives for the structural layer are

discussed and an architecture with only thin film structural layers is selected for further studies.

3.1 Studies on Electrode Architectures

As discussed in Section 2.3, IDE based cantilever type PEHs utilize the d_{33} coefficient, which is higher than d_{31} for most piezoelectric materials. IDE architecture has some additional advantages over PPE; first of all, the output voltage amplitude depends on the distance between the fingers as opposed to piezoelectric material thickness [37]. This is an important advantage for MEMS scale, where the piezoelectric material thickness is limited to several micrometers at best. Although increased voltage comes at the expense of reduced capacitance, an output voltage that can exceed diode turn on voltages is crucial if the generated energy is to be rectified and stored in a capacitor or battery. Furthermore, the fabrication process is simpler since only one electrode layer is required [37]. With all these advantages, IDE based PEHs can be viable candidates for energy harvesting at MEMS scale.

Figure 3.1 shows a sample IDE pattern with the parameters that define the electrode geometry; finger width w_e, finger spacing s_e, bus width w_{bus}, and finger-bus spacing s_{bus} [66]. As discussed in Section 2.3, IDE type PEHs need to be poled using the same IDEs that will be used to collect the generated charge. An analytical solution to the IDE pattern optimization for PEHs is not feasible due to the complex nature of the problem, which includes both the poling and harvesting steps. An alternative and reliable method is solving the problem numerically using FEM simulations. The effect of IDE geometry on the electric field distribution had been studied using FEM tools for actuators [85, 86] and energy harvesters [87].

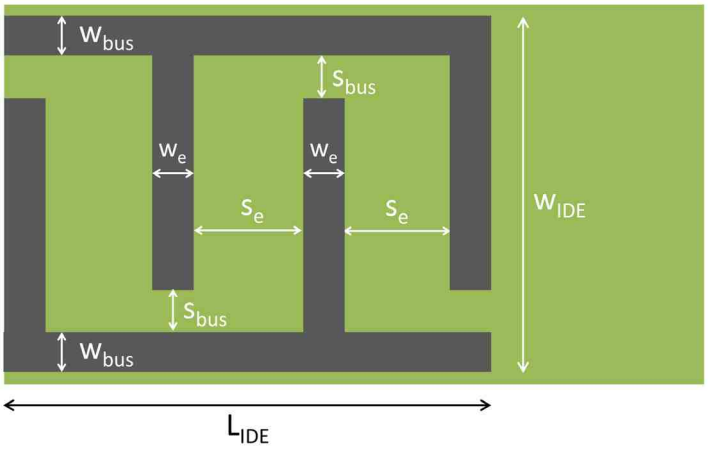
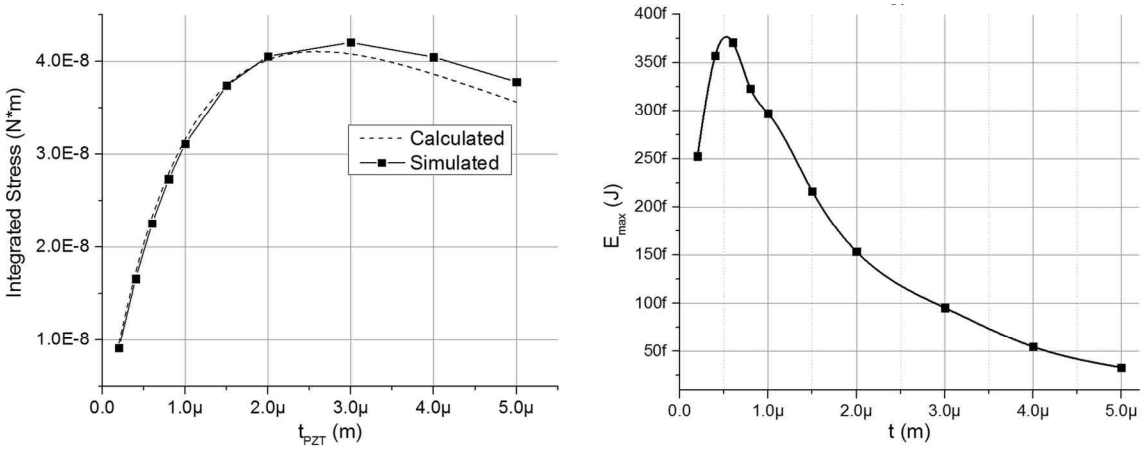


Figure 3.1: A sample IDE pattern with dimensions L_{IDE} by w_{IDE} that shows the parameters that define electrode geometry: finger width w_e, finger spacing s_e, bus width w_{bus}, and finger-bus spacing s_{bus} [66].

A comprehensive study on the effect of IDE pattern and piezoelectric layer thickness on energy harvesting performance was performed during the course of this thesis work [66]. The study proposed a 2-stage FEM simulation method for the geometry optimization of IDE based PEHs; first stage to calculate the average polarization orientations of certain regions within the piezoelectric material, which are then used in the second stage simulations to calculate the electrical energy generated in response to a stationary force [66]. The proposed method was demonstrated on a sample MEMS scale PEH model using COMSOL Multiphysics [66]. One of the interesting results of this study was about the optimum PZT layer thickness. Figure 3.2 (a) shows the volume integral of the longitudinal stress in the piezoelectric material due to a 15 μN tip force for various thickness values, which shows an optimal value around 3 μm [66]. On the other hand, electrical energy output values obtained from the FEM simulations show a much lower optimal thickness value as shown in Figure 3.2 (b) [66]. This result is attributable to the geometrical structure of IDE type devices, where electrodes are placed only on one

side of the piezoelectric material. The effect of the electric field generated by a piezoelectric material region on the overall electrical output depends on its distance to the electrodes. Therefore, the utilization efficiency of the piezoelectric material drops as its thickness is increased in IDE type devices [66]. As a result of this conclusion, the focus of the study was shifted to PPE type PEHs, which can utilize the entire volume of the piezoelectric material between the electrodes.



(a) **(b)**

Figure 3.2: (a) The volume integral of the longitudinal stress in the piezoelectric layer due to a 15 μN tip force for various thickness values [66]. (b) Simulated electrical energy output of the same device in response to the same tip force [66]. Maximum electrical energy was obtained at a much lower thickness value, indicating that the piezoelectric material utilization efficiency is lower in thicker films.

3.2 Piezoelectric Material Comparison

Most of the reported MEMS scale PEHs utilize PZT as the active material since its strong piezoelectric properties help improve the overall energy conversion efficiency. However, deposition of piezoelectric thin film PZT is not a CMOS compatible process because of the high temperature thermal annealing step required for crystallization. A method to create CMOS compatible PEHs using PZT is bonding bulk the ceramic on

CMOS substrate and then grinding it to bring the thickness down to acceptable levels [34, 45]. However, required extra bonding layers and mechanical grinding process increase the complexity and fabrication cost. A material class that have even higher piezoelectric properties is relaxor ferroelectrics such as lead magnesium niobate-lead titanate (PMN-PT) [33]. Epitaxially grown thin film PMN-PT has been shown to exhibit much stronger piezoelectricity than even bulk PZT [92]. However, fabrication of these films also require high temperature annealing steps that cannot be applied on substrates that contain CMOS circuits [92].

The studies on CMOS compatible PEHs are mostly focused on AlN, which can be deposited using sputtering at temperatures lower than 400 °C [58]. A similar piezoelectric material, which has also Wurtzite structure and can be deposited with sputtering at low temperatures, is ZnO. The piezoelectric coefficients of the two materials are also similar; however, the number of reported AlN based MEMS scale PEHs is much higher than ZnO based devices. The CMOS compatibility of these devices comes at the cost of reduced electromechanical conversion factors compared to PZT films [34]. Furthermore, both AlN and ZnO have higher elastic modulus values, which means that for a given device geometry and resonance frequency, ZnO or AlN films have to be thinner than PZT films.

Another class of potentially CMOS compatible piezoelectric materials is piezoelectric polymers. Although piezoelectricity is observed in a large number of polymers, PVDF and its copolymer PVDF-TrFE are the most widely used ones. Both polymers exhibit similar mechanical and piezoelectric properties [93]. However, PVDF-TrFE has a significant advantage for MEMS applications; unlike PVDF, it does not require mechanical stretching in order to induce piezoelectricity [93, 94]. PVDF-TrFE

crystallizes into its piezoelectric β phase when annealed at a temperature between its Curie temperature and melting temperature [93]. These temperatures depend on the molar ratio of VDF and TrFE in the copolymer; but are lower than 200 °C in any composition [95]. Piezoelectric properties also depend on the molar ratio; Ohigashi et al. discovered in 1982 that copolymers with 70-80% VDF molar ratio have electromechanical coupling factors as high as 0.3 [93, 95]. This value is higher than that of sputter deposited AlN, which was reported as 0.23 by Dubois et al. [96].

Although the electromechanical coupling factors are not significantly different, PVDF-TrFE has certain advantages over AlN. First of all, PVDF-TrFE is a soft material with low elastic modulus like most polymers. As a result, it would be possible to coat thicker piezoelectric layers for a given PEH device geometry and resonance frequency [69]. This in turn would increase the power output, which is proportional to the volume of the piezoelectric material. Fabrication of thicker layers is also much easier and inexpensive for PVDF-TrFE, which can be deposited via spin coating from its solutions in various inexpensive solvents such as methyl ethyl ketone (MEK) or dimethylacetamide (DMAc). Thickness of the layer can be easily and accurately adjusted by modifying the polymer concentration in the solution and spin coating parameters. The easy fabrication method also enables creating multiple electrode-polymer layers [97-101]. This can be used to adjust the electrical impedance of the PEH for a given total piezoelectric layer thickness in order to obtain better matching to the harvesting circuit. Another advantage of PVDF-TrFE is its flexibility; it can accommodate much higher strains compared to brittle ceramics without breaking. This property increases the reliability of the PEH by reducing the risk of fracturing in case of impacts or other high acceleration sources [70].

Furthermore, it increases the maximum allowable power output, which is proportional to the strain on the piezoelectric material. Nakajima et al. investigated the performance of PVDF under high mechanical strain and showed that the piezoelectric charge output was linear up to at least 0.4% strain, a strain much higher than what PZT can withstand without breaking [102]. The authors calculated that for strains higher than 0.8%, power output of PVDF films would exceed the maximum that can be obtained from PZT blocks with the same volume [102]. It should be noted that the authors calculated this for bulk PZT-5H; therefore, PVDF, and similarly, PVDF-TrFE could provide higher power density even at lower strains in case of thin films. Finally, piezoelectric polymers have low mechanical Q factors, which lead to a wider bandwidth for a given mechanical structure [103]. Although low Q factor reduces the maximum attainable power in case of reduced external damping such as vacuum packaging, a more flat frequency response allows easier mechanical and electrical design.

Due to the most salient advantages listed above, PVDF-TrFE was considered as a potential candidate for the targeted high performance CMOS compatible MEMS PEHs. An FEM study was performed using COMSOL Multiphysics in order to investigate the energy harvesting performance of PVDF-TrFE and compare it to other prominent piezoelectric materials [69]. Figure 3.3 shows the output voltage and power values obtained from the simulations of 2-dimensional MEMS scale PEH models utilizing PVDF-TrFE, AlN, and ZnO [69]. The thickness values of the piezoelectric materials were selected to result in the same neutral axis location when deposited on top of a 2 μm-thick SiO_2 structural layer. The results show that the energy harvesting performance of PVDF-TrFE is comparable to ZnO and significantly higher than AlN [69].

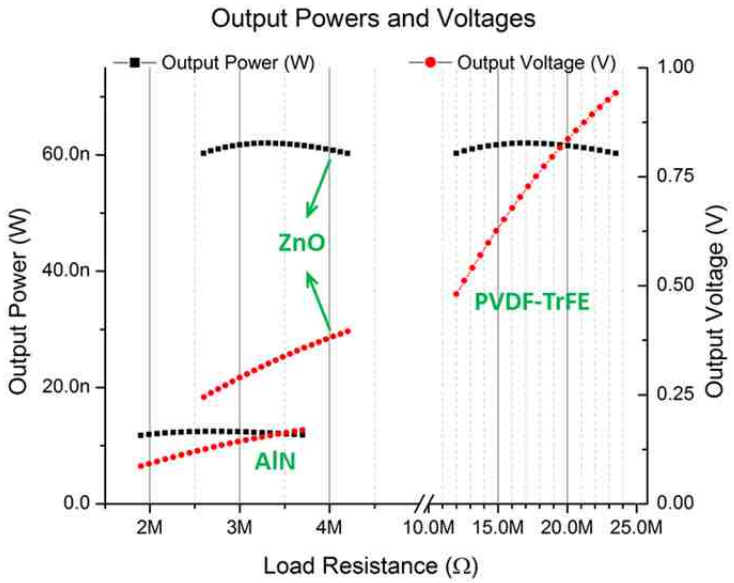


Figure 3.3: Output voltage and power values obtained from the FEM simulations of 2-dimensional MEMS scale PEH models using PVDF-TrFE, AlN, and ZnO [69]. Thickness values of the materials were selected to give the same neutral axis location with a 2 µm-thick SiO_2 structural layer.

Figure 3.3 shows that the optimal load resistance of PVDF-TrFE based device is much higher compared to the others. The reason is its lower capacitance; the low elastic modulus of PVDF-TrFE allows the deposition of a thicker layer, which reduces the capacitance by increasing the electrode distance. Nevertheless, simple fabrication process of PVDF-TrFE offers a possible method to adjust the PEH impedance while keeping the total piezoelectric material constant by forming multiple electrode/piezoelectric layers. The examination of this multiple layer approach via FEM simulations showed that the multiple layer approach do not degrade the output performance of the device [69].

3.3 Structural Layer Selection

A typical MEMS scale PEH consists of structural, piezoelectric, and electrode layers. As discussed in Section 2.3, the structural layer is an important part of the PEH design; it

provides mechanical sturdiness to the device, and in case of unimorphs, it is necessary in order to move the neutral axis outside the piezoelectric material. Figure 3.4 shows three different structural layer options for MEMS scale cantilever type PEHs; (a) device and buried oxide layers of silicon-on-insulator (SoI) wafers, (b) thin films with partially etched bulk Si underneath, and (c) only thin films with the bulk Si completely etched.

(a) **(b)** **(c)**

Figure 3.4: Structural layer options for MEMS scale PEHs: (a) Device and buried oxide layers of SoI wafers, (b) Thin films with partially etched bulk Si underneath, and (c) Thin films with the bulk Si completely etched.

One of the popular choices for structural layer is the device layer of silicon-on-insulator (SoI) wafers, which is formed by etching the handle layer from back side and using the buried oxide as an etch stop [42-45]. This method forms a single-crystal structural Si layer with a precisely controlled thickness, which enables accurate mechanical design for intended operation mode and frequency. In addition, relatively thick and robust single-crystal Si layer increases the mechanical reliability of the device and allows utilization of thick piezoelectric layers. However, this method limits the potential monolithic integration of PEHs to SoI CMOS ICs, which are typically used only for special applications due to their higher cost.

It is possible to obtain a similar layer structure on standard Si wafers by time-controlled etching of the bulk Si [38, 47, 48]. This method can bring the robust and thick

structural layer advantage of SoI wafers to standard Si wafers, which are much more commonly used for CMOS ICs. However, achieving a uniform Si thickness with time-controlled etch is difficult since the rate and uniformity of the etch processes depend on numerous factors, including the dimensions of the etch openings.

The third option, which is illustrated in Figure 3.4 (c), is creating a structural layer that is comprised of only thin films, which allows a consistent and accurate control over the layer thicknesses [37, 46]. PEHs fabricated with this method can be monolithically integrated with any kind of CMOS IC by using the isolation and passivation layers as structural layers. Furthermore, resonance frequency will be lower since equivalent spring constant of a suspended layer decreases with decreasing thickness. However, there are two main drawbacks of using thin films as structural layers for PEHs. First of all, suspended thin films can be extremely fragile, which reduces the reliability of the PEHs. The other drawback is the reduced maximum piezoelectric layer volume in case of cantilever type PEHs; the efficiency will drop if the piezoelectric layer is thick enough to encompass the neutral axis, along which the sign of the strain changes. Nevertheless, using PVDF-TrFE as the active material alleviates both problems. The elastic modulus of the polymer is much lower compared to commonly available MEMS thin films such as SiO_2 and Si_3N_4; therefore, it is possible to deposit a thick piezoelectric layer without reducing the efficiency. Furthermore, the thick and flexible polymer layer deposited on the thin structural layers increases the robustness of the device.

CHAPTER 4: CHARACTERIZATION OF PVDF-TRFE THIN FILMS

Characterization of the piezoelectric material is a critical step of PEH design. There are studies in the literature reporting the dielectric, ferroelectric, and piezoelectric properties of PVDF-TrFE films with various thicknesses and molar compositions [77, 93, 95, 104, 105]. However, these properties also depend on process conditions, especially at macro scale. Therefore, thin film PVDF-TrFE coating process was optimized to obtain high quality films, details of which are discussed in the next section. The dielectric, ferroelectric, and piezoelectric properties of the fabricated high quality films of 75/25 molar ratio PVDF-TrFE films were measured. The measurements were performed on simple parallel plate capacitor structures illustrated in Figure 4.1. The thickness of the PVDF-TrFE film used for the characterization studies was measured as 1.3 μm using a TENCOR Alpha-Step 200 profilometer.

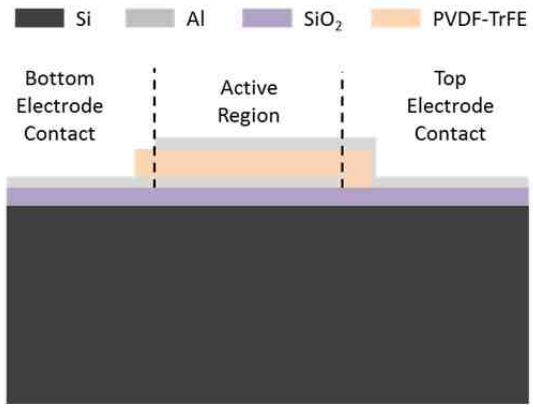
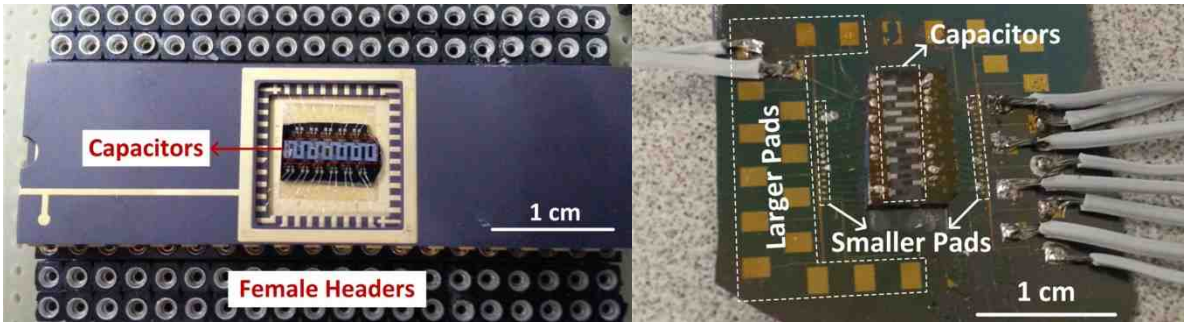


Figure 4.1: Cross-sectional view of the PVDF-TrFE capacitors used for characterization studies.

The dielectric and ferroelectric properties of the film were measured using a Radiant Precision Premier II ferroelectric tester. The piezoelectric measurements were done using

Piezo Nano Displacement System (PNDS), which is the combination of the ferroelectric tester with a tabletop atomic force microscope (AFM). Two different packaging methods were used for these characterization tests. Figure 4.2 (a) shows a sample with PVDF-TrFE capacitors wire bonded to a standard DIP40 IC package. This packaging was the nominal choice due to its reliability, low parasitic capacitance, and standard connection pattern. Therefore, it was used for dielectric measurements and ferroelectric measurements at room temperature. However, the piezoelectric measurements necessitate the sample fit under a tabletop AFM, which was not possible with the DIP40 package. In order to overcome this problem, a custom sample holder with lithographically created bonding pads was designed and fabricated on SiO_2 coated Si wafers. Figure 4.2 (b) shows a sample wire bonded to one of these custom sample holders. These thin holders with flat surfaces allow easy temperature control using a hot plate as well. Therefore, in addition to piezoelectric measurements, this packaging was used in temperature dependent ferroelectric measurements as well.



(a) **(b)**

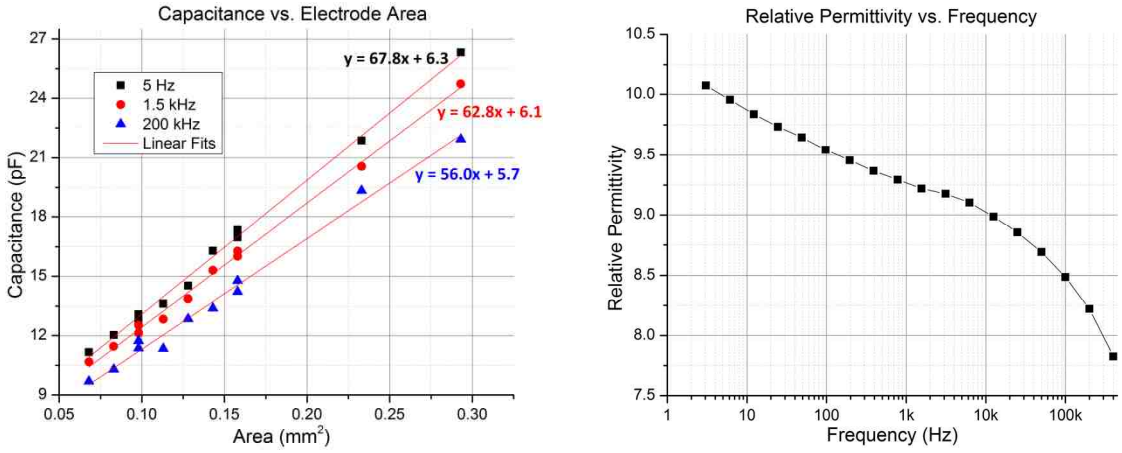
Figure 4.2: (a) PVDF-TrFE capacitors wire bonded to a standard DIP40 IC package used for the dielectric measurements and ferroelectric measurements at room temperature. (b) PVDF-TrFE capacitors from the same wafer that are bonded to a custom-made silicon wafer piece with lithographically created pads. These capacitors were used for piezoelectric and high temperature ferroelectric tests.

4.1 Dielectric Measurements

Dielectric characterization is one of the requirements to create an electrical model for the PEH, which is inherently a capacitive device. At low frequencies up to MHz range, most capacitors can be modeled as a parallel combination of an ideal capacitor in parallel with a resistor, which models the losses. The values of both the capacitor and the resistor in this model are usually frequency dependent. Therefore, the capacitance and dielectric loss factors of the test samples were measured at different frequencies.

Capacitance measurements were performed on multiple capacitors with different electrode areas bonded on the same DIP40 package. Unit area capacitance of the PVDF-TrFE film was then extracted from the linear fits of these measurements. Figure 4.3 (a) shows the capacitance values measured at 5 Hz, 1.5 kHz, and 200 kHz from capacitors with electrode areas ranging from 0.07 mm^2 to 0.29 mm^2 [106]. Linear fit lines and corresponding equations are also shown in the figure. The slope and *y*-intercept of these equations should give the unit area capacitance and parasitic capacitance in the setup, respectively. For example, unit area capacitance of the PVDF-TrFE film and parasitic setup capacitance at 5 Hz can be directly seen as 67.8 pF/mm^2 and 6.3 pF, respectively. Relative permittivity can then be found by multiplying the unit area capacitance with the measured film thickness of 1.3 μm, which yields a relative permittivity of 10.0 at 5 Hz. This procedure was applied to the measurement results at various frequencies from 3 Hz to 400 kHz. Figure 4.3 (b) shows the relative permittivity values calculated from these measurements [106]. Relative permittivity was observed to decrease logarithmically with a slope of 0.32/decade with increasing frequency, reaching 9.0 at 12.5 kHz. The reduction slope increases further after that point, yielding a relative permittivity of 7.8 at 400 kHz.

Nevertheless, such high frequencies are irrelevant for vibration energy harvesting; the low frequency range with the constant logarithmic slope is the main region of interest.



(a) **(b)**

Figure 4.3: (a) Capacitances measured at 5 Hz, 1.5 kHz, and 200 kHz from capacitors with electrode areas ranging from 0.07 mm^2 to 0.29 mm^2. Linear fits and corresponding linear equations are also shown [106]. (b) Frequency dependence of the relative permittivity of the PVDF-TrFE film as calculated from the capacitance measurements [106].

Dissipation factor of a capacitor can be defined as the ratio of the dissipated energy to the stored energy in each period of the applied signal. The losses in capacitors can occur within the dielectric by the mechanisms of resistive leakage and dielectric loss, as well as on the connectors due to their finite resistance. The former two mechanisms can be modeled with a resistor in parallel with the capacitor, while the latter is in series. Nevertheless, losses due to electrode resistance are usually negligible up to very high frequencies. Leakage and dielectric loss are more dominant at low and mid-range frequencies, respectively and hence more relevant for vibrational PEHs. Figure 4.4 shows the dissipation factor measurement results of PVDF-TrFE capacitors at a frequency range from 1.5 Hz to 100 kHz [106]. Solid lines in the graph show data from 3 individual capacitors, whereas the dashed line shows averaged data of 11 capacitors. Relatively flat

low frequency end of the curves indicate that the contribution of leakage is almost negligible even at frequencies as low as 1.5 Hz. Consequently, electrical energy dissipation within the PEHs will be almost completely due to dielectric loss. The average dielectric loss was measured to be less than 0.5% for frequencies up to 1 kHz, after which it increases almost quadratically with increasing frequency. Nevertheless, with a value less than 1.5% even at 50 kHz, dielectric loss is not expected to be a major source of inefficiency in the PEHs.

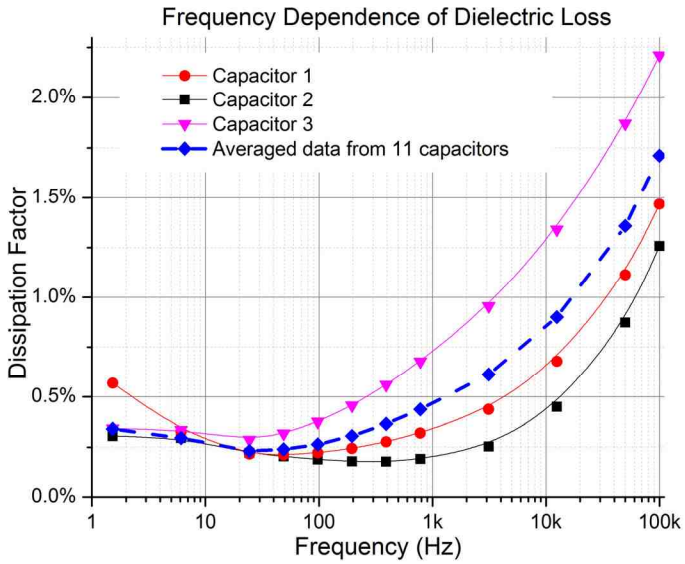


Figure 4.4: Dissipation factors of PVDF-TrFE capacitors measured at different frequencies [106]. Solid lines show measurements from 3 different capacitors, whereas the dashed line shows the average data from 11 capacitors.

4.2 Ferroelectric Measurements

Ferroelectric materials belong to crystal groups that exhibit spontaneous polarization within their unit cells. This polarization can be reversed by the application of a strong external electric field. Once switched, the direction of the spontaneous polarization is retained unless a sufficiently strong electric field is applied in the opposite direction. This

unique property of ferroelectric materials leads to hysteresis in their voltage-polarization curves, which is basically a line for linear dielectrics. Figure 4.5 illustrates this process on a sample electric field-polarization curve exhibiting hysteresis. A pristine ferroelectric sample starts from the origin and follows path 1 as the field is increased. As the electric field becomes strong enough to align the dipoles inside the crystals, the slope of the curve increases, which corresponds to path 2 in the figure. After all dipoles are aligned, the curve saturates and follows path 3. As the electric field is decreased, polarization curve follows path 4, reaching a non-zero value at zero electric field. Same phenomenon occurs in the negative cycle of the curve as well, and the loop is closed by path 8 joining path 2. The curve cannot return to path 1 unless the polarization states of the material are reset by heating it over its Curie temperature. The *x*-intercept and *y*-intercept of this curve are called remnant polarization and coercive field, respectively.

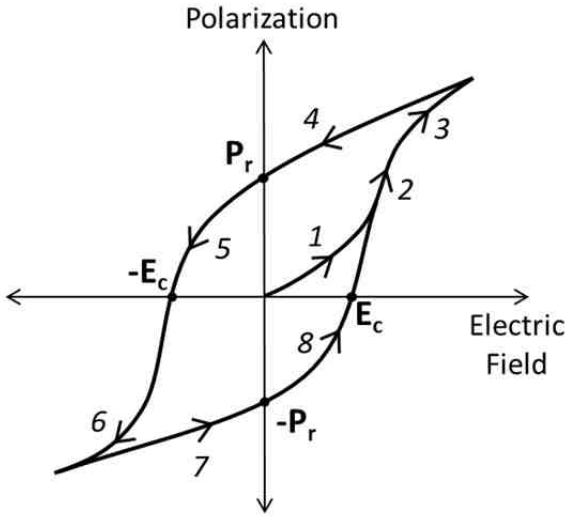


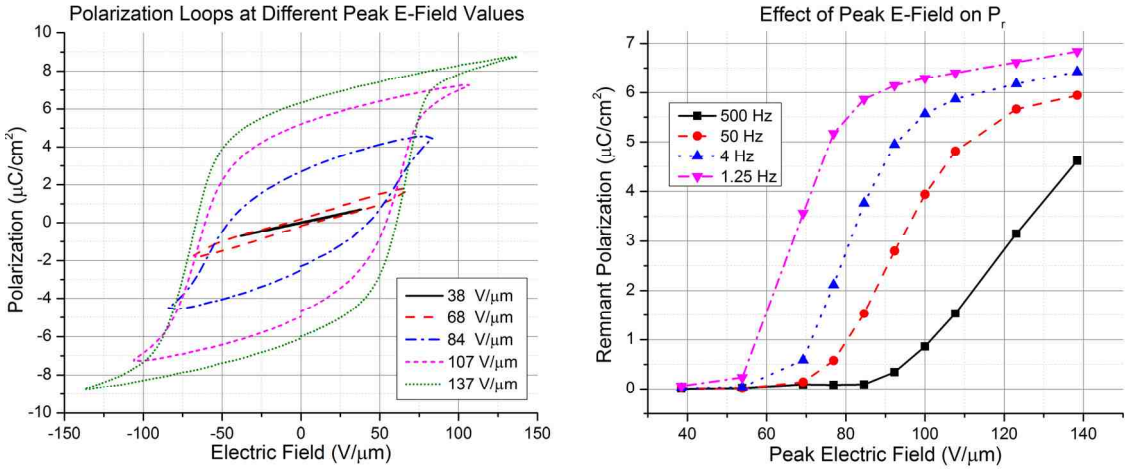
Figure 4.5: A sample ferroelectric hysteresis curve, which initially starts from the origin and follows path 1. Steep slope around path 2 indicates the start of polarization alignment, followed by saturation region, path 3, with linear response. Removing the voltage moves the curve along path 4, yielding a remnant polarization P_r. Same response is obtained if a negative voltage cycle is applied, creating a closed hysteresis loop.

PVDF-TrFE is a ferroelectric material, which means that its polar axis can be reversed by sufficiently strong external electric fields. Ferroelectric materials are also utilized purely for this property, most prominently in non-volatile ferroelectric random access memories (FeRAM). In these devices, data is written to the memory by applying a strong electric field to set the polarization direction in the material, which is retained after the field is removed. Therefore, FeRAMs are expected to undergo frequent polarization state changes. On the other hand, the material is usually poled only once in piezoelectric devices after fabrication and retain the same polarization afterwards. As a result, dynamic ferroelectric properties are not as relevant in piezoelectric devices. However, some of the ferroelectric measurements can provide useful data on the required poling conditions or achievable operation temperature range for piezoelectric devices. To exemplify, higher remnant polarization implies stronger piezoelectric response, and coercive field values indicate the required poling voltages for similar thin films. Nevertheless, a comprehensive ferroelectric characterization of the film was performed for the sake of completeness. This chapter presents the results of this characterization study, which includes an examination of the dependence of polarization hysteresis loops on the waveform amplitude, waveform frequency, and temperature. The fatigue effect on the ferroelectric behavior due to repeated polarization switching was also examined.

4.2.1 Electric Field and Frequency Dependence at Room Temperature

Voltage-polarization loops of the capacitors were measured at room temperature using bipolar triangular waves with varying amplitude and frequencies in order to observe the effect of these parameters on the remnant polarization and coercive field of the fabricated film. Figure 4.6 (a) shows polarization loops obtained using 4 Hz bipolar

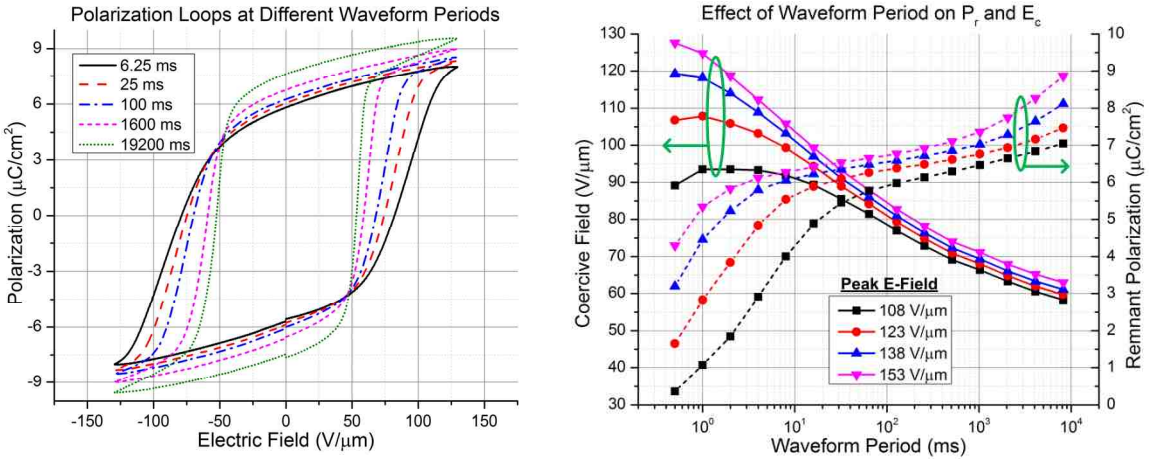
triangular waveforms with different peak amplitudes [106]. No hysteresis behavior was observed in the waveforms with peak electric field values of 38 V/μm and 68 V/μm, meaning that the coercive field is higher than 68 V/μm at 4 Hz. Remnant polarization in a ferroelectric material increases as the applied electric field is increased until it saturates. The saturation depends on the frequency of the input waveform as well. Figure 4.6 (b) shows the dependence of the remnant polarization on the peak electric field at different frequencies [106]. The saturation level of the remnant polarization for this specific sample was approximately 6.5 μC/cm^2. As expected, the saturation point shifts towards lower electric field inputs as frequency decreases. Consequently, a given remnant polarization can be achieved with lower electric fields at lower frequencies. However, there is a lower limit of coercivity in ferroelectric materials, under which there is no remnant polarization is observed regardless of the frequency [107]. This lower limit was found to be approximately 55 V/μm in the fabricated PVDF-TrFE films.



(a) **(b)**

Figure 4.6: (a) Polarization loops obtained using 4 Hz bipolar triangular waveforms with different peak amplitudes [106]. (b) Dependence of remnant polarization on the peak electric field for different frequencies [106]. No significant remnant polarization was observed under approximately 55 V/μm, regardless of the waveform period.

A similar set of measurements were performed in order to observe the effect of the waveform period on the ferroelectric behavior of the film. Figure 4.7 (a) shows polarization loops obtained using bipolar triangular waveforms with different periods. The remnant polarization increases only slightly with increasing waveform period, indicating saturation. On the other hand, coercive field shows a more significant change. Figure 4.7 (b) shows the effect of the waveform period on both remnant polarization and coercive field. As seen in the figure, coercive field decreases logarithmically with increasing period in the region where remnant polarization is already saturated. At the left end of the graph, the signal is too fast for a complete polarization switching, which is the reason of apparent reduction in the coercive field with decreasing period [108]. The apparent increase in the remnant polarization at the right side is due to the effect of resistive leakage.

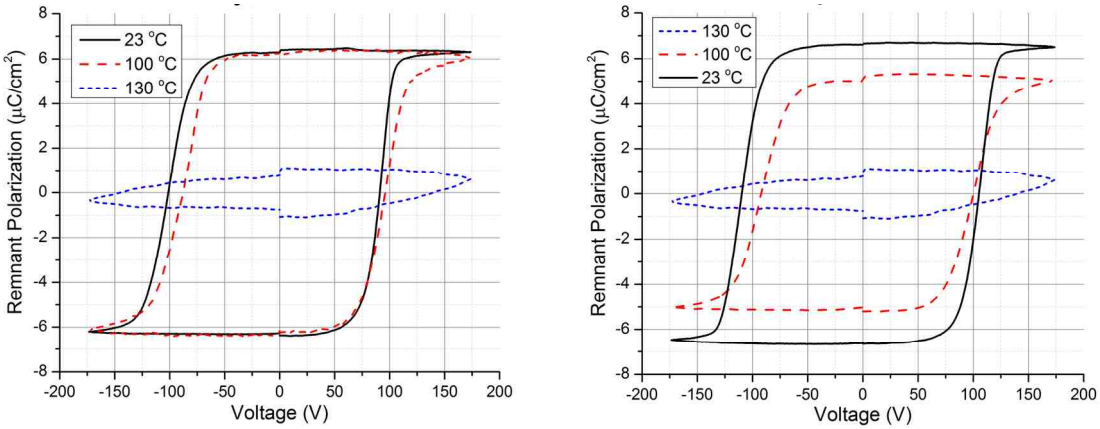


(a) **(b)**

Figure 4.7: (a) Polarization loops obtained using bipolar triangular waveforms with 130 V/μm peak amplitude and different periods. A slight increase in remnant polarization and more significant reduction in coercive field were observed with increasing period. (b) Effect of the waveform on the remnant polarization and coercive field. Coercive field decreased logarithmically with increasing period after the remnant polarization reaches saturation.

4.2.2 Temperature Dependence of Hysteresis

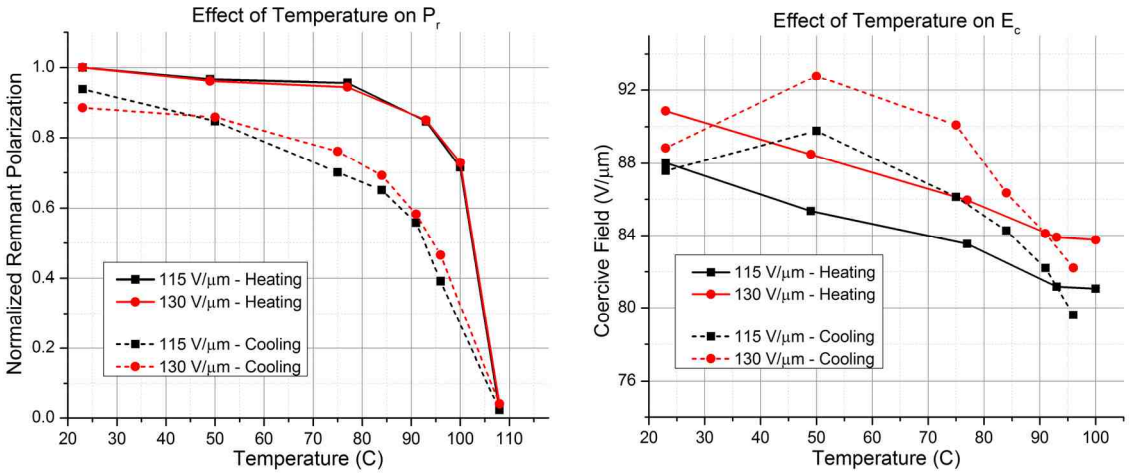
Temperature dependence of the ferroelectric response was examined between 23 °C and 130 °C. Sample temperature was set by a hot plate and a non-contact thermometer, and polarization loops were measured during both heating and cooling periods. Figure 4.8 shows remnant polarization loops measured from a capacitor during (a) heating and (b) cooling cycles using bipolar triangular waveforms with 350 ms periods. These loops were obtained using the automated remnant hysteresis measurement task of the ferroelectric tester, which makes multiple switching and non-switching measurements and calculates only the remnant part of the polarization. The almost non-existent remnant polarization at 130 °C indicates that the Curie temperature of the film has been exceeded. The well-known temperature hysteresis is also seen in the loops; the remnant polarization at 100 °C during cooling cycle is lower than the value measured at the same temperature during heating cycle.



(a) **(b)**

Figure 4.8: Remnant polarization loops obtained at different temperatures during (a) heating and (b) cooling cycles using bipolar triangular waveforms with 350 ms periods.

Figure 4.9 shows (a) normalized remnant polarization, and (b) coercive field at various temperatures during both heating and cooling cycles [106]. Remnant polarization shows a sharp reduction after 95 °C and reaches 108 °C upon heating. The restoration of the remnant polarization during cooling follows a different path, verifying the aforementioned temperature hysteresis. The slight loss in remnant polarization after the full heating/cooling cycle is probably due to ferroelectric fatigue, which is examined in detail in the next subsection. The coercive field also shows a dependence on the temperature; it decreases with a slope of -0.1 V/μm·K as temperature increases.



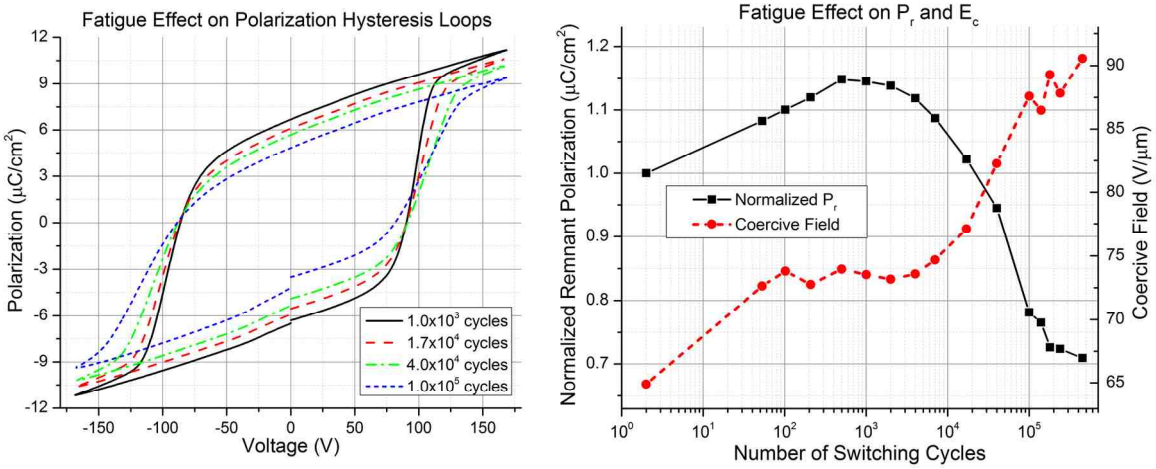
(a) **(b)**

Figure 4.9: (a) Normalized remnant polarization and (b) coercive field at various temperatures between 23 °C and 110 °C [106]. Solid and dashed lines show the heating and cooling cycles, respectively. Remnant polarization showed a sharp reduction after 95 °C and reaches zero at 108 °C. Coercive field slightly decreased with increasing temperature.

4.2.3 Ferroelectric Fatigue

Ferroelectric fatigue can be simply defined as the degradation of the hysteresis loops with repeated polarization switching in the material. The rate of the degradation depends on the shape, amplitude, and frequency of the applied switching voltage as well as the

temperature [109, 110]. The ferroelectric fatigue performance of the PVDF-TrFE film was measured at room temperature using 5 Hz bipolar triangular waveforms with a peak electric field of 130 V/μm. Figure 4.10 (a) presents polarization loops demonstrating the degradation in the ferroelectric characteristics of the sample after repeated polarization switching cycles. Figure 4.10 (b) shows the change in the remnant polarization and coercive field with increasing number of cycles. An initial enhancement period, during which both the remnant polarization and coercive field increases, was observed until the first 10^3 cycles are completed. This enhancement was hypothesized to be due to the increased degree of ordering in the interfacial layers [111, 112]. After this peak, a fast reduction in the remnant polarization and a concurrent increase in coercive field were observed, indicating degradation of ferroelectric behavior. Nevertheless, the degradation slowed down after 10^5 cycles; normalized remnant polarization was measured as 0.78 and 0.71 after $1.0x10^5$ and $4.5x10^5$ cycles, respectively.



(a) **(b)**

Figure 4.10: (a) Polarization loops showing the degradation in the ferroelectric behavior after repeated polarization switching cycles. (b) Change in the remnant polarization and coercive field with increasing number of cycles.

4.3 Piezoelectric Measurements

Piezoelectric characterization of the fabricated PVDF-TrFE film was performed using PNDS, a system designed to measure nanometer-scale piezoelectric displacements. It should be noted that displacement measurements on thin films give an effective piezoelectric coefficient, which is smaller than the actual coefficient due to the clamping by the rigid substrate [113]. Figure 4.11 (a) is a simplified schematic diagram showing the operation principle of this system [106]. In this system, an AC signal is applied to the sample by the ferroelectric tester after it is brought into contact with the AFM probe. Resultant piezoelectric displacement generates a proportional signal in the AFM detector by bending the probe, which is fed back to the tester for processing. Detector signal can be converted into displacement amplitude using the data obtained from force-distance curves of the AFM. The tester software automatically performs averaging and drift correction on the obtained data. Figure 4.11 (b) shows the photograph of the PNDS setup with a sample placed on the AFM chuck [106]. A close-up view of the sample and the probe before they are brought into contact is also shown in the inset.

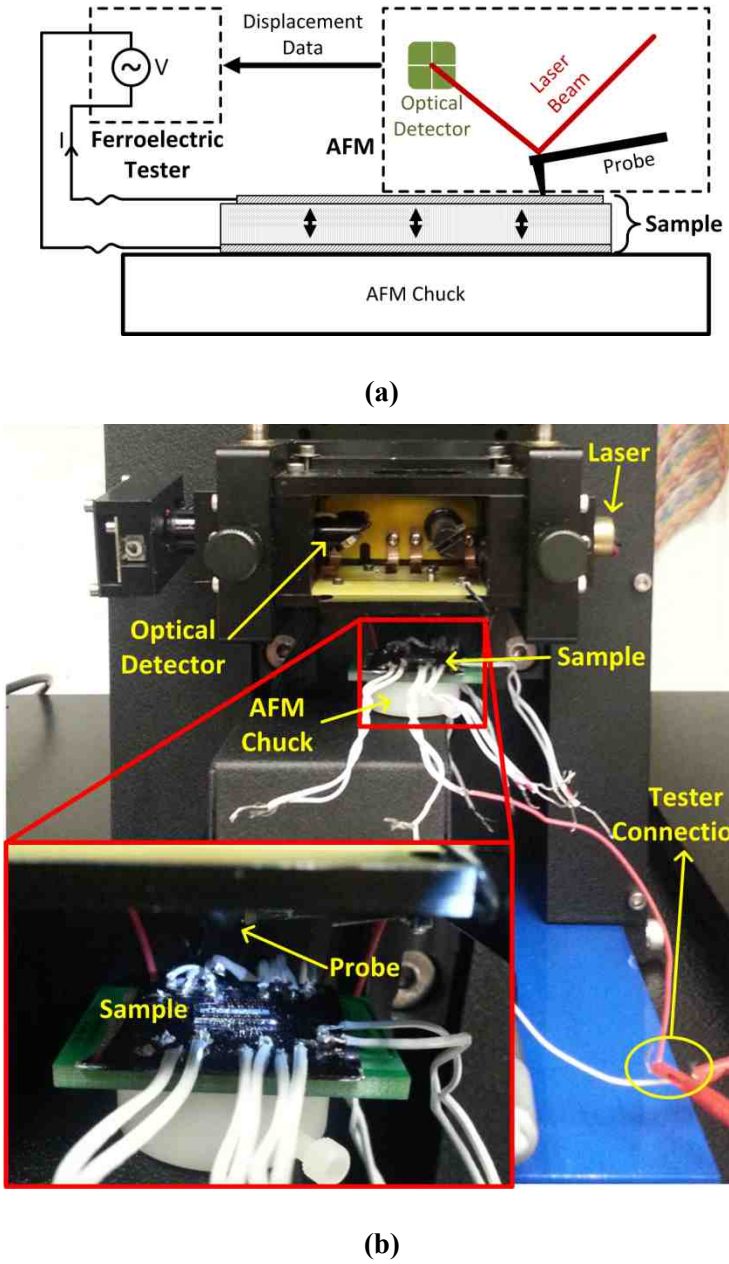


Figure 4.11: (a) Simplified schematic diagram showing the operation principle of PNDS [106]. Piezoelectric displacement in response to the AC signal creates a proportional signal in the AFM detector. (b) Photograph of the PNDS setup with a sample placed on the AFM chuck for measurements [106]. The inset shows the close-up view of the sample and AFM probe, which are brought into contact for measurements.

Figure 4.12 shows the piezoelectric displacement loops obtained using with waveforms with switching and non-switching characteristics [106]. Polarization switching waveforms, bipolar triangular waveforms with ±170 V peak, generate a typical

"butterfly loop", which is caused by the polarization reversal with the strong electric field. The polarization reversal inside the material quickly reverses the sign of the strain, after which a linear characteristic is observed. The same polarity and hence the linearity, is retained in the material until a similar input voltage amplitude is reached at the opposite polarity, causing the polarization to revert back. Non-switching waveforms were applied to the sample after the polarity was set to a certain direction. Voltage amplitudes were adjusted such that the polarization of the material is never reverted. In case of the non-switching waveforms, a linear relationship was observed between the applied voltage and resultant displacement. The slopes of the non-switching curves are equal to the effective d_{33} coefficients of the film in two reverse polarization directions.

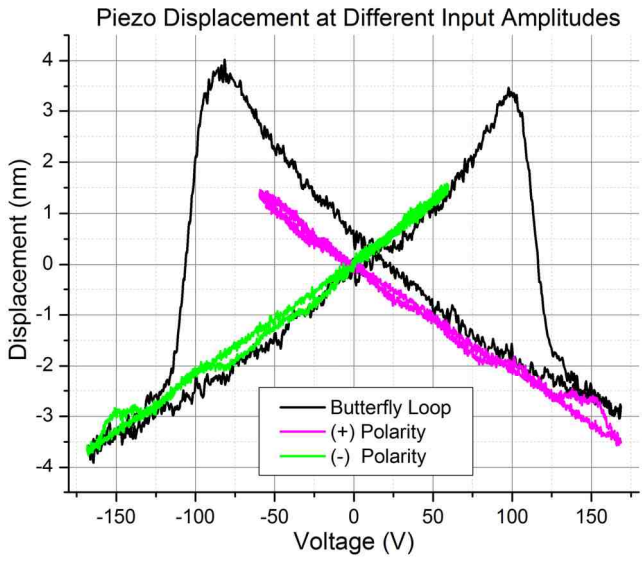
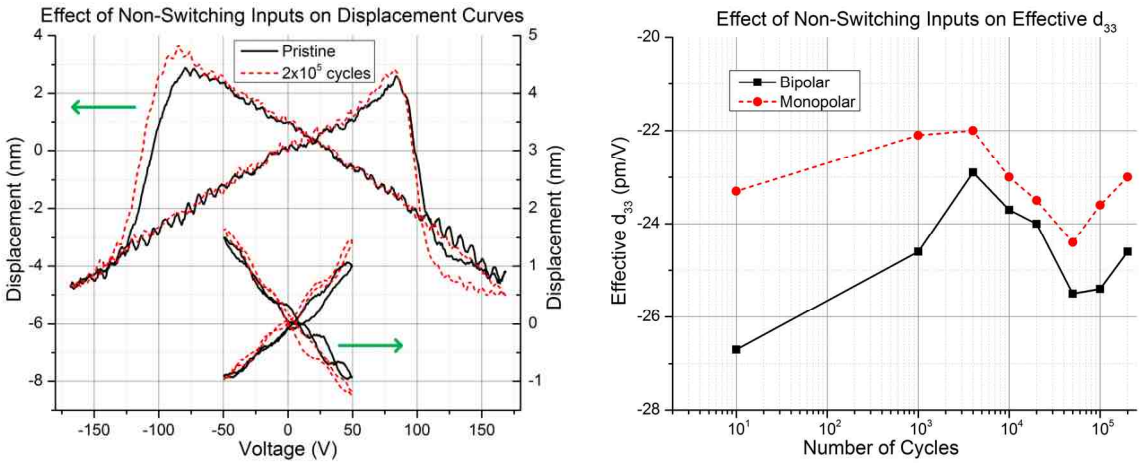


Figure 4.12: Piezoelectric displacement loops obtained using voltage waveforms with switching and non-switching amplitudes [106]. Switching waveforms generate "butterfly loops", showing the polarization reversal due to high electric field. Non-switching waveforms demonstrate a linear voltage-displacement relationship in both polarities.

Effective d_{33} measurements of the PVDF-TrFE film were performed using non-switching waveforms after the polarization is set using a DC electric field of 130 V/μm.

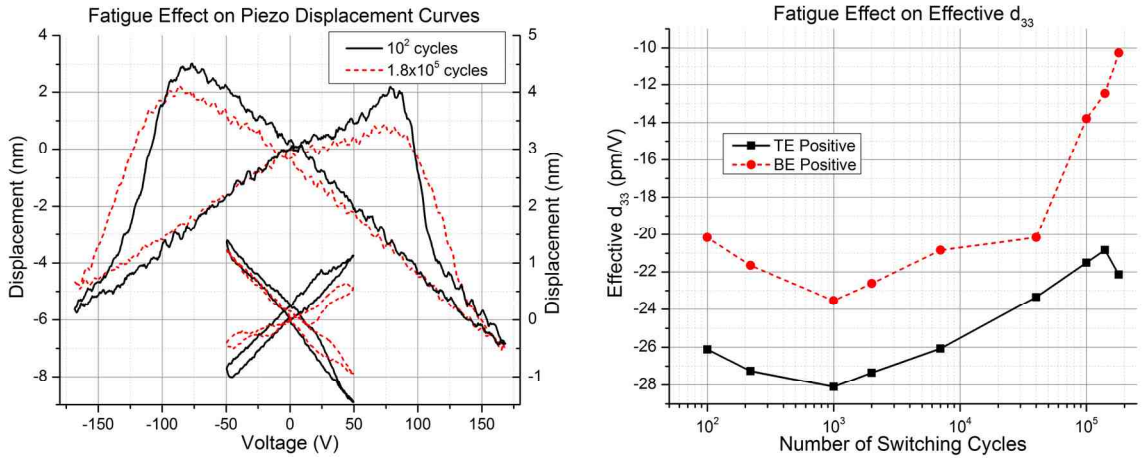
The effect of repeated non-switching input cycles was also examined by exciting the samples with non-switching waveforms at 5 Hz between measurements. Switching waveforms were only applied at the beginning and end of the measurements for comparison. Figure 4.13 (a) shows the switching and non-switching piezoelectric displacement curves obtained before the DC poling and after $2x10^5$ non-switching cycles [106]. No significant difference was observed between the measurements, except the increased negative coercive field due to imprint, which is consistent with the results previously reported in the literature [109, 114]. Figure 4.13 (b) shows the effective d_{33} values measured after various numbers of non-switching cycles [106]. The average value and maximum deviation of the effective d_{33} throughout this set of measurements were found as -23.9 pm/V and 15.4%, respectively.



(a) **(b)**

Figure 4.13: (a) Switching and non-switching piezoelectric displacement curves measured before DC poling and after $2x10^5$ non-switching cycles [106]. No significant difference was observed between the measurements, except the increased negative coercive field due to imprint. (b) Effective d_{33} values in response to 200 Hz unipolar and bipolar waveforms [106]. Maximum deviation in the effective d_{33} values throughout these measurements were found as 15.4%.

Effect of ferroelectric fatigue on the piezoelectric performance was also examined by a similar set of measurements. The sample was subjected to repeated polarization switching cycles between measurements using a 5 Hz bipolar triangular waveform with ±170 V amplitude. Figure 4.14 (a) shows the piezoelectric displacement loops for switching and non-switching input waveforms after 10^2 and $1.8x10^5$ polarization switching cycles [106]. Both large signal and small signal curves show significant degradation, indicating the fatigue effect on piezoelectric performance. Figure 4.14 (b) shows the effective d_{33} measured after various numbers of switching cycles [106]. Initial values were measured as -26.1 pm/V and -20.2 pm/V for downward and upward polarization, respectively. The coefficient exhibited an initial enhancement period of 10^3 cycles and started to degrade after approximately 10^4 cycles. Effective d_{33} decreased by 24% and 42% after $1.8x10^5$ cycles from their peak values for downward and upward polarizations, respectively.



(a) **(b)**

Figure 4.14: (a) Switching and non-switching piezoelectric displacement curves measured before DC poling and after $1.8x10^5$ switching cycles [106]. Both small signal and large signal curves show significant degradation. (b) Effective d_{33} values measured from non-switching waveforms at 200 Hz [106]. Effective d_{33} decreased by 24% and 41% after 10^5 cycles from their peak values for downward and upward polarizations, respectively.

CHAPTER 5: PROCESS DEVELOPMENT AND FABRICATION OF PVDF-TRFE BASED MEMS ENERGY HARVESTERS

A framework for the targeted PEH architecture was determined to maximize the electromechanical energy conversion efficiency while satisfying the CMOS compatibility requirement. Based on the preliminary studies presented in Chapter 2, unimorph cantilever with thin film structural layers is selected as the mechanical architecture, PVDF-TrFE is selected as the active material to be utilized, and PPE was selected as the electrode architecture. This section presents the experimental studies on the realization of the designed PEH prototypes. The next section lists the process development studies performed for high quality PVDF-TrFE piezoelectric thin films. The other section presents the fabrication and test results of the PEHs.

5.1 Process Development for PVDF-TrFE Thin Films

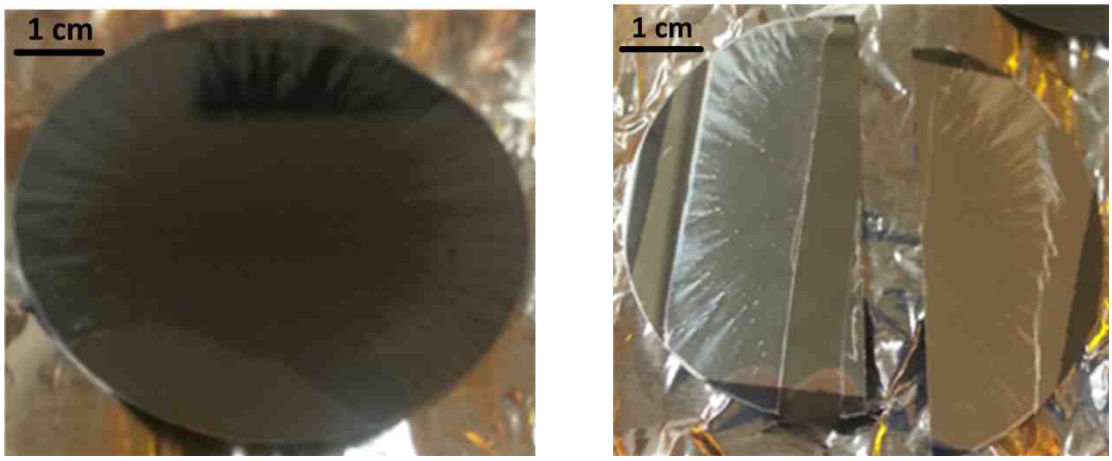
Most of the fabrication steps required for a cantilever type MEMS PEH are frequently used standard processes such as metal deposition by sputtering to form the electrodes, or bulk Si etching with high anisotropy by deep reactive ion etching (DRIE) to form the proof masses. However, piezoelectric materials are used only for specific applications in MEMS; therefore, fabrication steps involving the deposition and patterning of piezoelectric materials are not very well-established. On the other hand, process optimization of the piezoelectric material is essential for PEHs especially at MEMS scale, where small dimensions necessitate highly efficient designs in order to achieve reasonable power output levels. Therefore, initial studies were focused on optimizing the fabrication process of PVDF-TrFE.

The highest electromechanical coupling factor of the polymer, which is a critical parameter for energy harvesting applications, is reported to be highest for VDF molar ratios between 70% and 80% [93]. Therefore, PVDF-TrFE with a molar ratio of 75/25 was purchased from Solvay, Inc. in powder form. Solutions with different weight ratios were then prepared by dissolving the powder in methyl ethyl ketone (MEK) for spin coating. Spin coating is a well-known deposition method for PVDF-TrFE thin films. After the spin coating, the remaining solvent is evaporated first, which is usually done on hot plates. Then, the substrate is annealed to improve the crystallinity of the film. The annealing temperature has to be between the Curie temperature and melting temperature of the material [93]. There are no other certain requirements regarding the temperature or duration of these treatments although there are a number of studies on the optimization of these parameters [115, 116]. The methods reported in these studies were used as a basis for the process, which is later improved further by resolving the encountered problems. The following subsections discuss these problems and developed solutions.

5.1.1 PVDF-TrFE Film Uniformity Improvement

Despite the simplicity of the spin coating method, some problems were encountered during the initial experiments. In the very first experiments, the films were significantly non-uniform, easily noticeable even at macro scale. Figure 5.1 shows spin coated PVDF-TrFE films on 2” Si wafers (a) directly on bulk Si and (b) on a thin film Al layer. Both films had comet-like shapes with significantly non-uniform surfaces. This problem was initially thought to be caused by air bubbles formed in the PVDF-TrFE solution. Therefore, initial efforts were focused on eliminating possible air bubble sources or using spin speed and ramp parameters that would allow any microscopic bubbles to vanish.

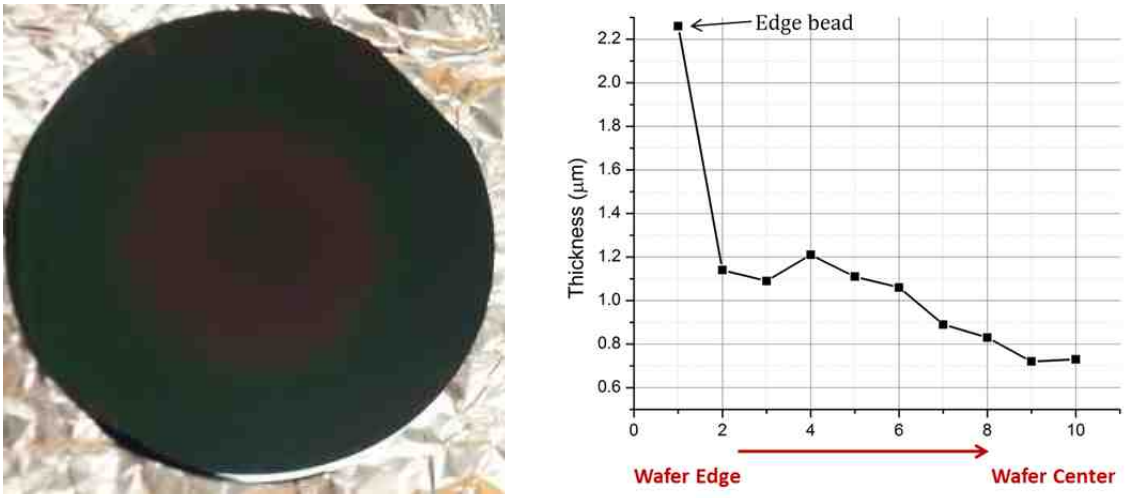
However, these efforts failed to eliminate the comet shapes, suggesting that they were not being caused by air bubbles.



(a) **(b)**

Figure 5.1: Spin coated PVDF-TrFE films on 2" Si wafers (a) directly on bulk Si, and (b) on top of a thin film Al layer during initial experiments. Both films had comet-like shapes with significant non-uniformity in the film surface.

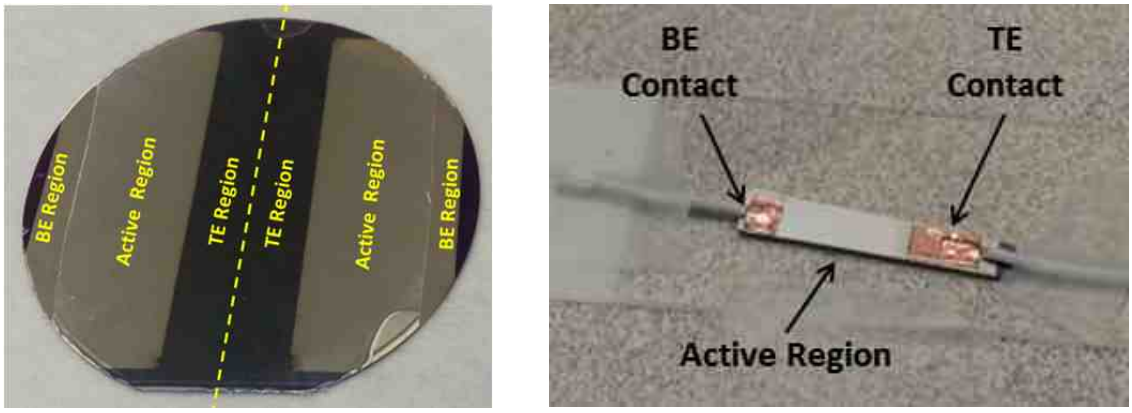
Another possible source for the comet-like shapes is relatively large particles inside the solution that obstructs the flow during spin coating. In order to test this hypothesis, the solution was filtered using quantitative filter papers and cell strainers with pore sizes ranging from 11 μm to 40 μm. Figure 5.2 shows (a) a 4" Si wafer with a PVDF-TrFE film spin coated from a filtered solution. A cut was then formed on this film from the wafer edge to the center using a razor for thickness measurements. Figure 5.2 (b) shows the results of these thickness measurements. A significant thickness difference was observed between the central and outer regions of the wafer. This non-uniformity, which was found to be caused by the bending of the wafer by the vacuum of the spin coater, is also the reason for the color difference observed on the wafer. This problem was solved in later experiments by taping a dummy wafer under the actual wafer.



(a) **(b)**

Figure 5.2: (a) 4" wafer with a PVDF-TrFE film spin coated from a filtered solution. (b) Thickness measurement results obtained along a line from the center of the wafer to the edge. The thickness difference between the middle and outer regions is the cause of the color difference on the wafer.

After the macroscopic quality of the PVDF-TrFE films were improved, simple devices were fabricated using shadow masks in order to test the ferroelectric properties of the fabricated films without doing lithography. Figure 5.3 (a) show a SiO_2 coated 2" Si wafer with sputter coated Al bottom electrode and spin coated PVDF-TrFE layers. Both layers were patterned by using vacuum tapes as shadow masks, and the wafer was annealed at 140 °C for 2 hours to improve crystallization rate. A second Al layer coated through another shadow mask was used to form PVDF-TrFE capacitors with separate top electrode and bottom electrode contact regions as shown in the figure. After top electrode patterning, the wafer was manually diced with a scriber into individual test samples. Figure 5.3 (b) shows one of these samples with cables attached to its electrodes using conductive copper tapes for ferroelectric tests. Preliminary ferroelectric measurements, which merely aimed to verify the presence of ferroelectricity, were performed using these samples.



(a) **(b)**

Figure 5.3: (a) 2" SiO_2 coated Si wafer with Al and PVDF-TrFE layers. Al layers were deposited by sputtering through vacuum tapes used as shadow masks. A second Al layer was deposited on top of the PVDF-TrFE to create capacitors with separate contact regions for top and bottom electrodes. (b) A sample prepared using this method with wires connected to its electrodes for ferroelectric tests.

The ferroelectric behavior of the fabricated PVDF-TrFE films were successfully verified using these simple prototype capacitors. However, several sparks were observed on the film during the ferroelectric measurements on these samples. These sparks not only disrupted the ferroelectric data due to sudden current bursts, but also damaged the samples and rendered them useless after a few hundred polarization switching cycles. Figure 5.4 shows two polarization hysteresis loops measured on the same sample. One of the loops has a discontinuity near the negative voltage peak, which indicates that a sparking occurred at that instant. The other loop was obtained immediately after that and it has a normal shape, indicating that the spark was not strong enough to cause a catastrophic damage in the film. However, this was not the case in most of the experiments; and therefore, the reason behind this problem was investigated in order to develop a solution.

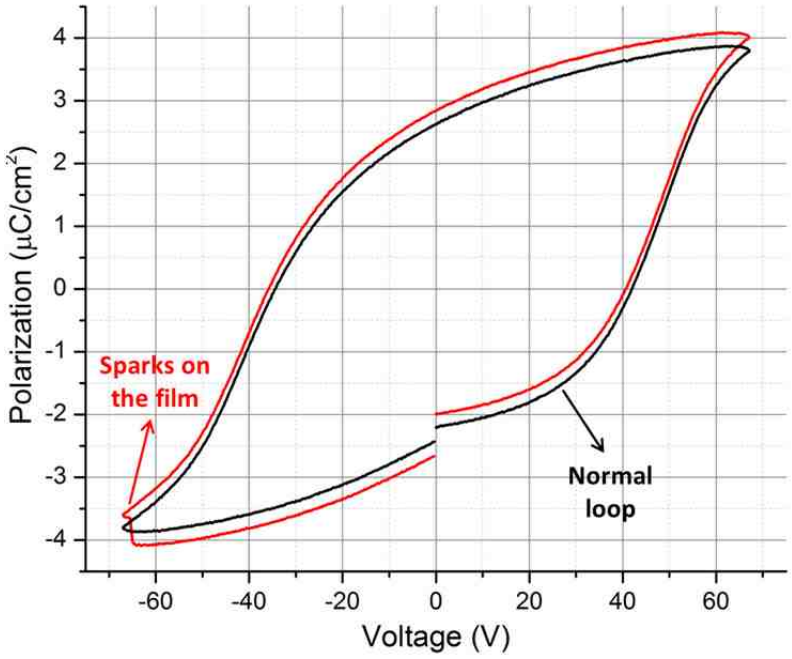
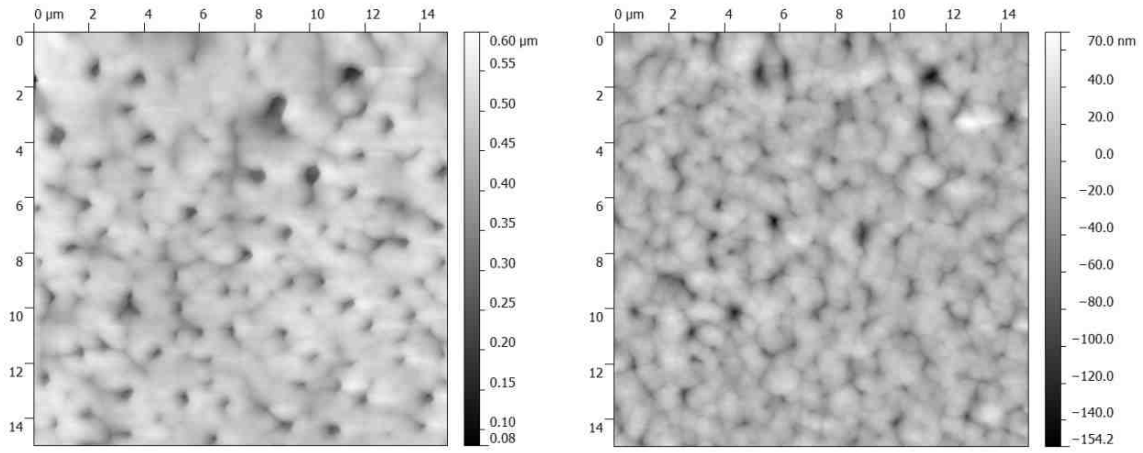


Figure 5.4: Two polarization hysteresis loops measured on the same sample. One of the loops has a discontinuity near the negative peak voltage, which is caused by sparking.

The most probable reason for the observed sparks was the existence of microscopic holes and non-uniformities, which can cause very high localized electric fields. This hypothesis was tested and verified by obtaining AFM images of the PVDF-TrFE surface. A possible solution proposed to alleviate this problem is adding an extra spin coating step using a dilute solution [117]. This process is hypothesized to improve the film uniformity by eroding the bumps and filling the holes on the film surface [117]. Figure 5.5 shows AFM images of PVDF-TrFE films deposited in (a) single step from a solution with PVDF-TrFE by weight, and (b) two steps, from 5% and 2% solutions by weight, respectively. The reduction in the density of the pinholes by the 2-step coating method can be seen by comparing these two images. The surface roughness values were measured as 72 nm and 21 nm for the single step and 2-step coated films, respectively.

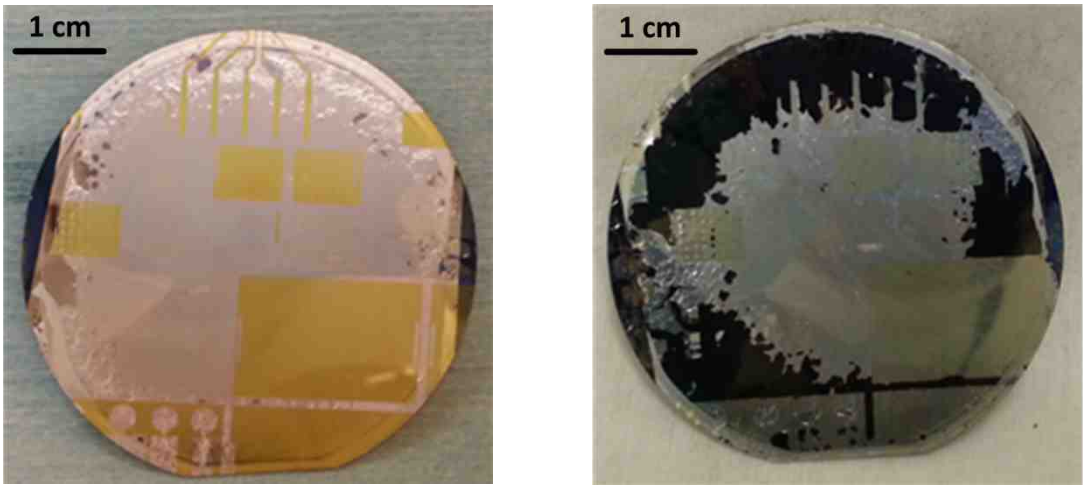


(a) **(b)**

Figure 5.5: AFM images of spin coated PVDF-TrFE films deposited in (a) single step using a solution with 5% PVDF-TrFE by weight, and (b) two steps from 5% and 2% solutions by weight, respectively. Surface roughness values were measured as 72 nm and 21 nm for single step and two step coatings, respectively.

5.1.2 Top Electrode Adhesion to PVDF-TrFE

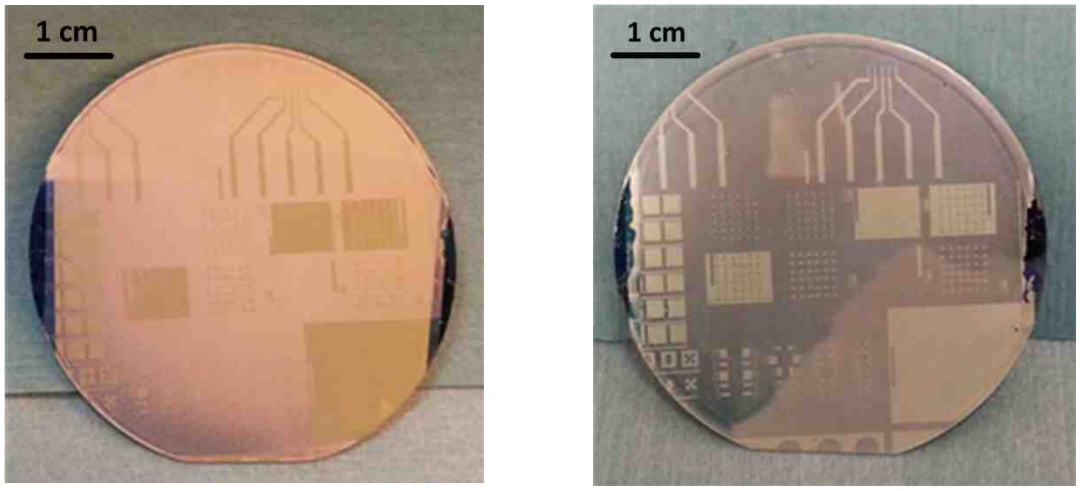
Initial experiments to verify the ferroelectric behavior of the deposited films had been done with crude fabrication methods as described in the previous section. During these tests, a weak adhesion was observed between the Al top electrode layer and PVDF-TrFE film; nevertheless, the metal films proved sufficient for these preliminary tests. However, weak electrode adhesion caused much more serious problems during lithography experiments. Large scale peeling was observed in the Al top electrode layers during photoresist develop phase, which destructed almost all features on the photoresist pattern. Utilization of a thin Ti adhesion layer reduced but did not eliminate the peeling problem. Figure 5.6 shows two PVDF-TrFE coated wafers with Ti/Al top electrodes after photoresist development, where (a) swelling and (b) peeling was observed.



(a) **(b)**

Figure 5.6: (a) Swelling and (b) peeling of a Ti/Al top electrode layer after photoresist development.

After the adhesion layer approach failed, PVDF-TrFE layer was considered to be causing the problem. One possible explanation was the outgassing, which is a known issue in polymers. As a potential solution, the annealing duration of the PVDF-TrFE films was increased to 3 hours before top electrode deposition. Figure 5.7 shows the results of the top electrode patterning experiments for (a) Ti/Al and (b) Cr/Al layers on 3-hour annealed PVDF-TrFE films. Both metal stacks were patterned without any problems, proving that the weak metal adhesion problem was at least partly due to insufficient thermal annealing of the polymer. This is an interesting result since it showed that the thermal annealing is necessary not only to improve the crystallinity, but also to improve electrode adhesion.



(a) **(b)**

Figure 5.7: Top electrode patterning experiment results for (a) Ti/Al and (b) Cr/Al layers on 3-hour annealed PVDF-TrFE films. Both metal stacks were patterned without any problems.

After the necessity of sufficient thermal annealing for good electrode adhesion has been observed, new experiments were run with Al electrodes on top of PVDF-TrFE consisting of lift-off and etch experiments. When the patterning was done via lift-off, which means that there was no Al film on the wafer during photolithography, no significant problems were observed. On the other hand, significant developer attack was observed when the patterning was done by etching. Figure 5.8 shows a photograph taken from a wafer with an Al film coated on top of PVDF-TrFE after photoresist develop. Although it has been known that most photoresist developers attack Al, the extent was substantially higher than normal in this case. In addition to the highly non-uniform Al attack visible at macro scale, it was also observed that thin (2 – 5 μm) lines were destroyed as soon as the develop process is completed. After these final experiments with Al electrodes, it was concluded that they can be used only if the patterning will be done by lift-off; a thin adhesion layer such as Ti or Cr is necessary otherwise.

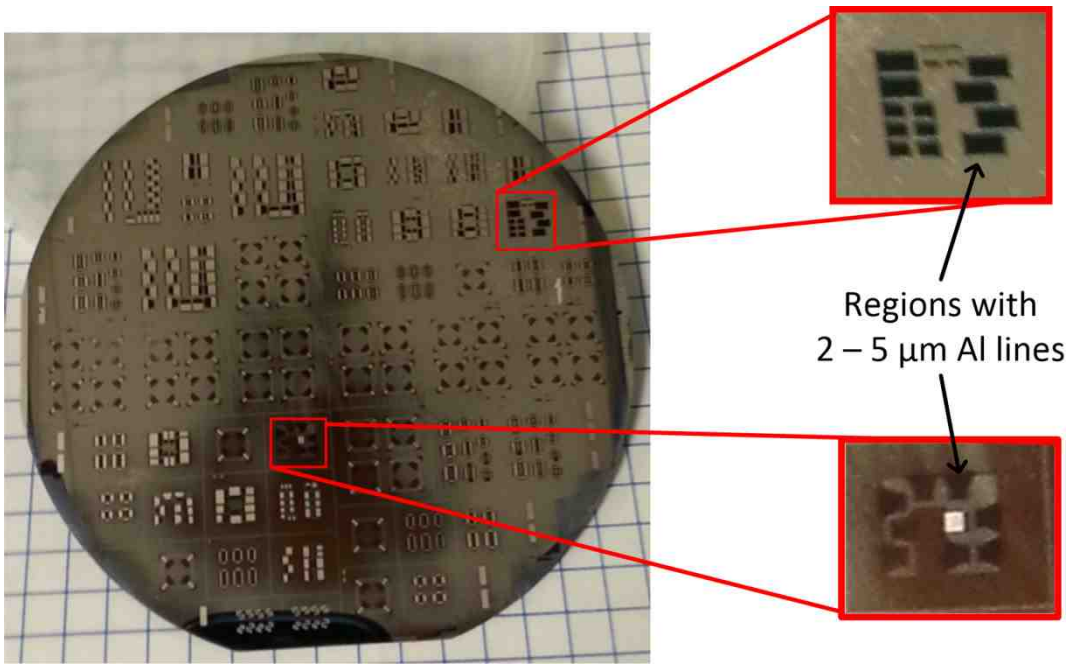


Figure 5.8: Photographs taken from a wafer with an Al film coated on top of PVDF-TrFE after photoresist develop. Highly non-uniform Al attack by the developer was clearly visible to bare eye. Thin patterns with 2 – 5 µm Al lines were completely destroyed.

5.2 Fabrication and Testing of PVDF-TrFE Based MEMS Energy Harvesters

Two generations of MEMS scale PVDF-TrFE based PEHs were fabricated during the course of this dissertation work. The first set of devices were fabricated using a single PVDF-TrFE layer with a sub-optimal thickness value in order to develop a complete process flow, fabricate proof-of-concept devices, and evaluate the energy conversion performance of the polymer at MEMS scale. Despite some problems, these first generation devices were successfully fabricated, and electromechanical energy conversion performances were verified by push-and-release tests. Second generation devices were designed with an optimized piezoelectric layer thickness. Instead of a single thick layer, PVDF-TrFE was coated as 3 thinner layers adding up to the same total thickness in the second generation devices. Multilayer approach not only provides

advantages for electrode continuity, but also allows higher capacitance per unit area, which makes impedance matching easier for maximum power transfer. Following sections describe the design, fabrication, and experiment results of both the single-layer first generation and multilayer second generation PEHs.

5.2.1 Proof-of-Concept PEHs with Single PVDF-TrFE Layer

The first generation of CMOS compatible PEHs with PVDF-TrFE was fabricated on a 4" Si wafer coated with 800 nm-thick low stress LPCVD silicon nitride (SiN_x) and 150 nm-thick PECVD SiO_2 layers. Figure 5.9 shows the process flow used to fabricate these devices [70]. In summary, PVDF-TrFE layer was deposited by spin coating and patterned by reactive ion etching (RIE) with O_2, top and bottom electrodes were deposited by sputtering and patterned by wet etching, bonding pads were formed with a lift-off process, and suspension of the cantilevers were performed with a DRIE step followed by a XeF_2 gaseous etch. The details of all fabrication steps can be found in the related publication [70].

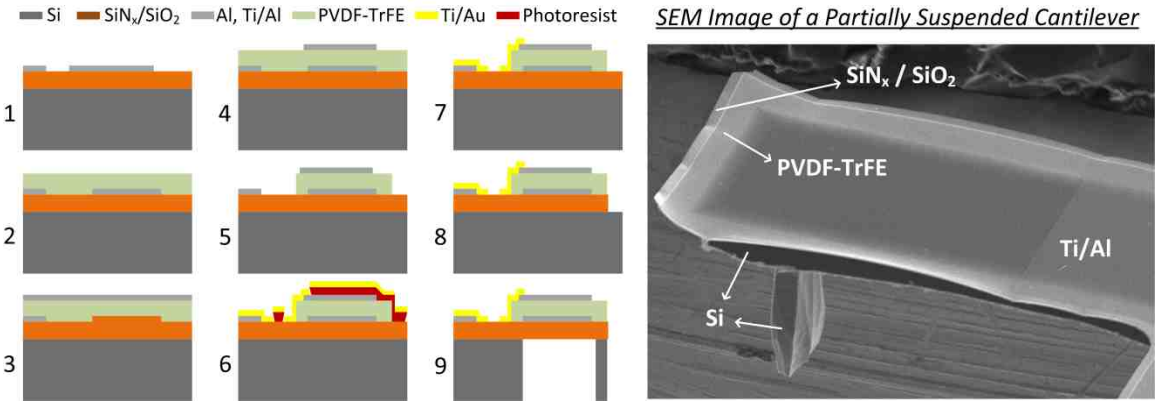


Figure 5.9: Process flow used to fabricate first generation PEHs [70]: (1) Sputtered and patterned Al bottom electrode, (2) spin coated PVDF-TrFE, (3) sputtered and (4) patterned Ti/Al top electrode, (5) patterned PVDF-TrFE, (6) patterned photoresist and sputtered Ti/Al for bonding pads, (7) formed bonding pads with lift-off, (8) patterned SiN_x and SiO_2, and (9) released cantilevers with backside DRIE and XeF_2 etch.

Using the described fabrication process, cantilevers with dimensions ranging from 300 μm to 2 mm were fabricated. Theoretical calculations using the elastic moduli values for the materials suggested that up to a 6 μm-thick PVDF-TrFE layer could have been deposited while keeping the neutral axis outside [70]. However, an upper limit of 1.5 μm was determined for PVDF-TrFE thickness for some practical reasons, and the actual thickness of the layer was measured as 1.3 μm after fabrication [70]. These practical issues were addressed for the second generation devices, which utilized much larger piezoelectric material volume per unit area.

After the fabrication, polarization hysteresis loops of the capacitors on suspended cantilevers were measured in order to verify the existence of ferroelectric behavior. Average remnant polarization and coercive field values were measured as 6.1 $\mu C/cm^2$ and 74.9 V/μm for a 4 Hz bipolar triangular input waveform with a peak voltage amplitude of ±175 V [70]. After the ferroelectric behavior was verified, cantilevers were poled at room temperature using DC bias voltages up to 200 V [70]. Energy harvesting performance of the cantilevers was then evaluated with push-and-release type measurements using a probe station. Figure 5.10 shows the photo of the measurement setup, which consists of a probe station, a custom-made probe-tip, a unity gain buffer circuit, a DC power supply, and an oscilloscope [70]. Using the custom made probe tip attached to the micropositioner of the probe station, PEH tips were pushed down and suddenly released, causing the cantilever to oscillate. Resultant voltage waveforms were then recorded and fit to damped sine wave equations in order to extract the amplitude, damping factor, and frequency information [70].

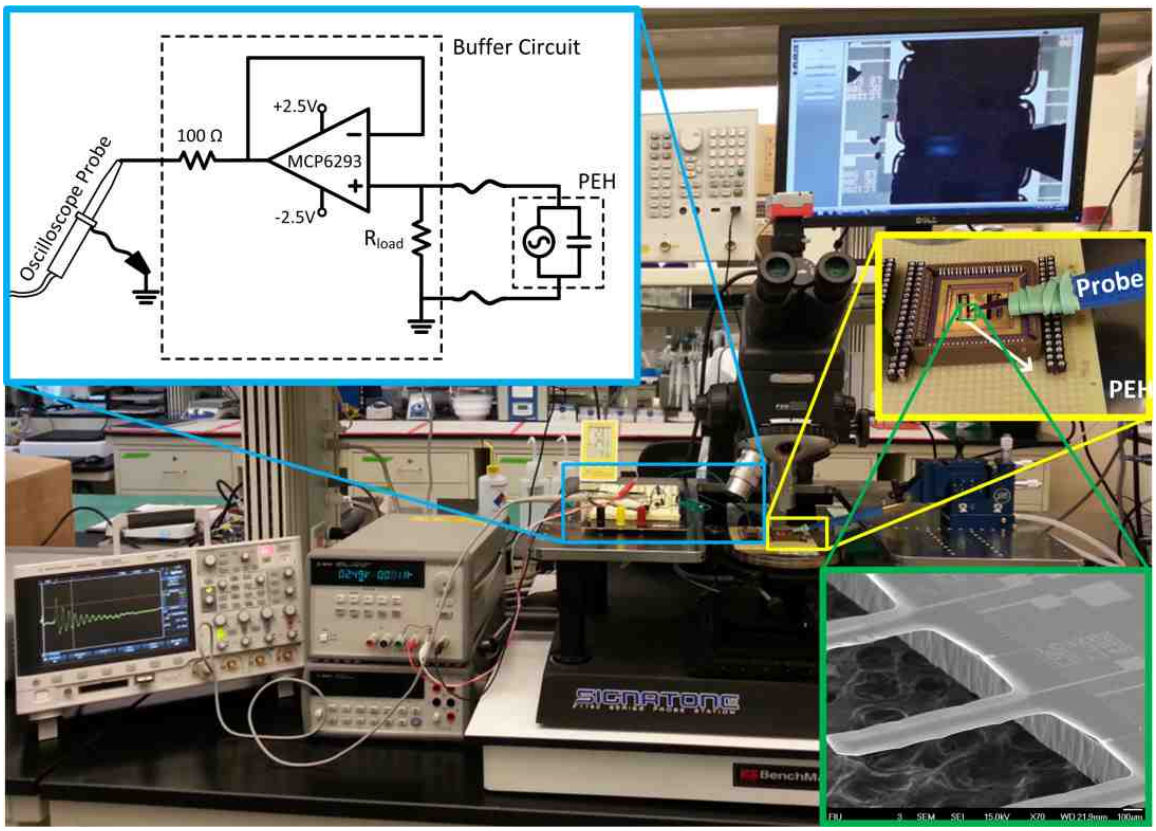
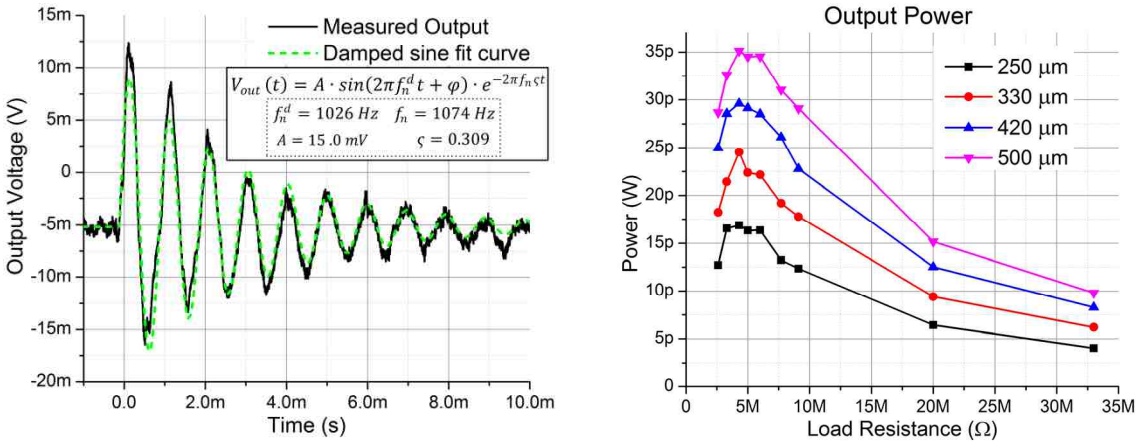


Figure 5.10: Photo of the measurement setup used to evaluate the energy harvesting performance of the fabricated devices [70]. The setup includes a probe station, a custom-made probe tip, a unity gain buffer circuit, a DC power supply, and an oscilloscope. Insets show the schematic of electrical connections in the setup, a close-up photo of the custom-made probe tip on top of a PEH, and an SEM image of the fabricated PEHs.

The push-and-release measurements were performed for different resistive load and tip displacement values. Figure 5.11 (a) shows the voltage generated by a 1200 μm × 300 μm cantilever with a resistive load of 5 MΩ in response to an initial tip displacement of 330 μm [70]. Curve fit to a damped sine wave yields an amplitude of 15.0 mV, damping factor of 0.309, and damped and undamped natural frequencies of 1026 Hz and 1074 Hz, respectively. Corresponding output power levels for harmonic displacements with the same tip displacement amplitudes were calculated from these parameters obtained from fit curves. Figure 5.11 (b) shows the calculated output power levels of the

same cantilever for different resistive loads [70]. The maximum power output was obtained with 4.3 MΩ load resistance for all displacement values, which corresponds to a power density value of 97.5 pW/mm^2 for a harmonic tip displacement with a 500 µm amplitude [70].



(a) **(b)**

Figure 5.11: (a) Voltage output of a 1200 µm × 300 µm cantilever measured on a 5 MΩ load in response to an initial tip displacement of 330 µm. Damped sine wave fit curve and extracted parameters are also shown [70]. (b) Calculated output power values of the same cantilever for different resistive loads and initial tip displacement values. Maximum power output density for a 500 µm harmonic tip displacement was calculated as 97.5 pW/mm^2 on a 4.3 MΩ load [70].

5.2.2 Optimized PEHs with Multiple PVDF-TrFE Layers

First generation of the PEHs proved useful for process development, film characterization, and proving the energy harvesting capability of PVDF-TrFE on MEMS scale devices. However, measured power output density was relatively low, mainly due to the sub-optimal PVDF-TrFE thickness. An upper limit of 1.5 µm had been determined during the design phase for two critical reasons: First of all, electrode continuity along high vertical walls of PVDF-TrFE would pose a problem due to non-conformal metal

coating process. The SEM image presented in Figure 5.12 illustrates this problem. The image shows a zoomed-in view of an electrode contact region along PVDF-TrFE edge. Relatively poor step coverage of physical vapor deposition (PVD) processes lead to small film thicknesses along vertical edges, yielding unreliable contact regions as seen in the figure. The other critical reason was the high voltage requirement; poling PVDF-TrFE at room temperature necessitates electric fields as high as 100 V/μm [116]. Consequently, poling films thicker than a few micrometers requires access to high voltage setup and equipment, which was not a feasible option. Addressing these issues was the first and foremost step of developing second generation PEHs with higher power output levels.

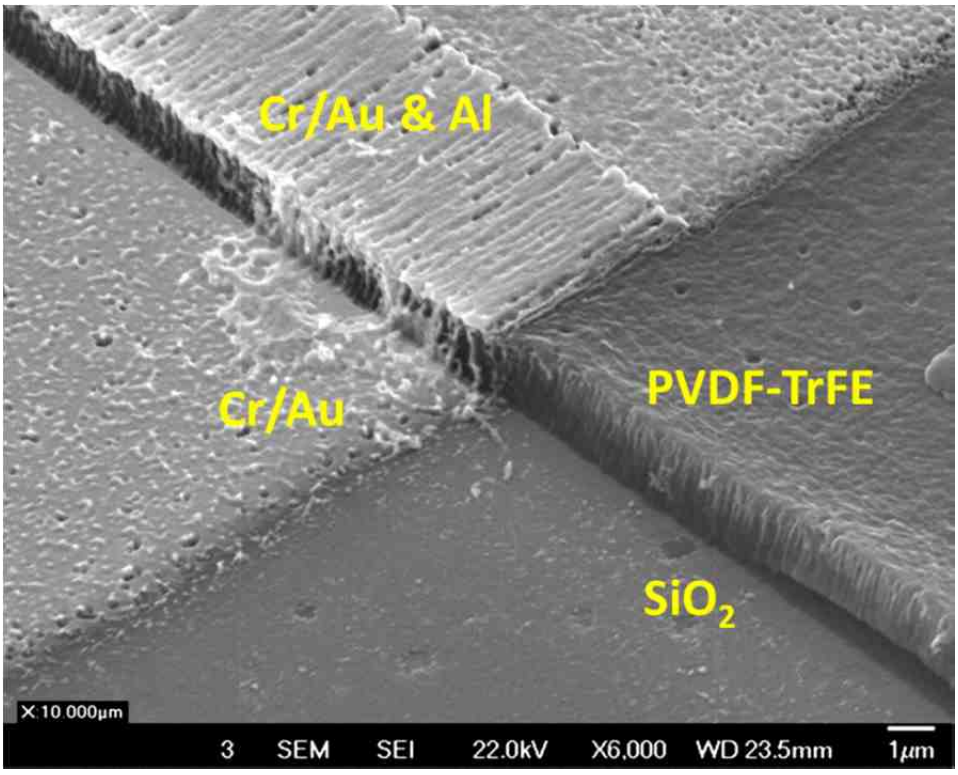
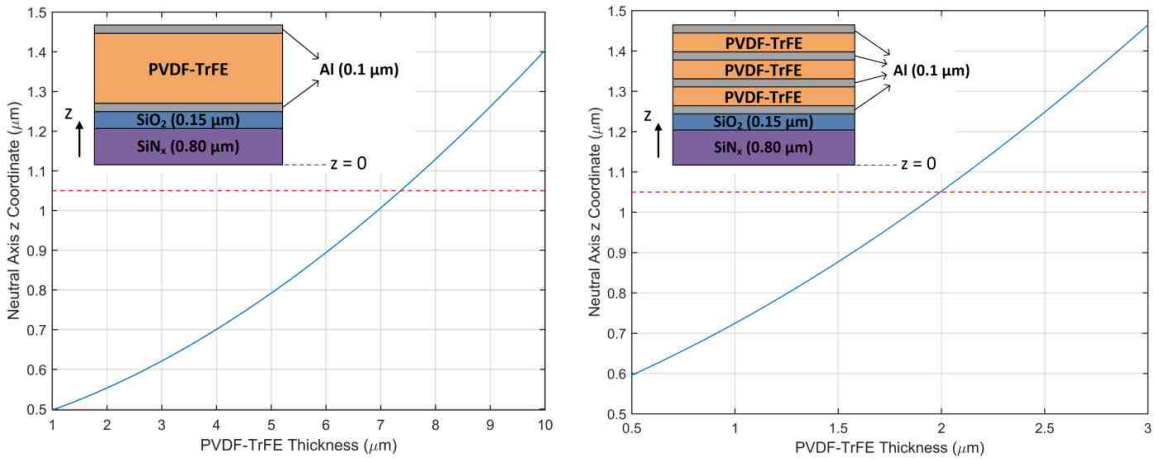


Figure 5.12: SEM image taken from a first generation PEH showing an electrode contact along PVDF-TrFE edge. Poor step coverage at the vertical walls yields unreliable contacts.

A possible solution to the discussed problems is using multiple piezoelectric-electrode layers to increase the total piezoelectric material thickness. As discussed before, simple fabrication process and low crystallization temperature of PVDF-TrFE allows fabrication of multilayer structures [101]. Furthermore, multilayer architecture can be used to adjust the PEH capacitance for a given total piezoelectric layer thickness, which can be useful for impedance matching for optimal power transfer [69]. Because of these reasons, a multilayer architecture was chosen for the second generation PEHs.

In the first step of the design phase, the substrate was chosen as the same 4" Si wafers coated with low-stress SiN_x (800 nm) and SiO_2 (150 nm) films, which constituted the structural layers. Then, dependence of the neutral axis location on piezoelectric layer thickness was examined for single-layer and 3-layer designs. Figure 5.13 shows the results of these calculations for (a) single-layer and (b) 3-layer structures as depicted in the insets. For the calculations, electrodes were chosen as 100 nm-thick Al layers. Elastic moduli were taken from literature for all the materials in the PEH structure; 295 GPa for SiN_x [118], 60 GPa for SiO_2 [119], 70 GPa for Al [120], and 3.7 GPa for PVDF-TrFE [77]. The dashed lines indicate the boundary between the first electrode and piezoelectric layers. This boundary was used to determine the maximum thickness for PVDF-TrFE, since a neutral axis inside the piezoelectric layer leads to charge cancellation as explained in Section 2.3.



(a) **(b)**

Figure 5.13: Neutral axis location for different PVDF-TrFE layer thickness values for (a) single-layer and (b) 3-layer designs. Total active layer thicknesses resulting in a neutral axis at the bottom boundary of PVDF-TrFE are 7.4 µm and 6.0 µm, respectively. The difference is caused by the mechanical effect of the electrode layers.

Maximum total PVDF-TrFE thicknesses for the single-layer and 3-layer structures according to the neutral axis criterion were found as 7.4 µm and 6.0 µm, respectively. The reason for this difference is the mechanical effect of two extra Al electrode layers in the latter. However, instead of sacrificing the piezoelectric material thickness for the multilayer design, a simple approach was chosen to keep the same thickness as the single-layer design. For this purpose, a spacer layer was planned to move the piezoelectric layer boundary up, which has essentially the same effect as using thicker structural layers. The material for the spacer layer was also chosen as PVDF-TrFE due to its simple fabrication process and small elastic constant. It can be calculated that only a 0.25 µm-thick spacer layer is sufficient in case of 2.45 µm PVDF-TrFE layer thickness, which yields the same total piezoelectric material volume as the single layer structure. Nevertheless, the thickness of the spacer layer was chosen as 0.5 µm to have a certain margin in the design.

After the target layer thicknesses were determined as 2.45 μm and 0.5 μm for the active and spacer PVDF-TrFE layers, respectively, a range was determined for the length of cantilevers. The criterion used to determine this range was the resultant resonance frequency. Undamped resonance frequency of a multilayer cantilever can be calculated using equations (2.19), (2.20), and (2.21). Equation (2.19) shows that the equivalent spring constant depends on the thickness and elastic constants of the layers as well as the width and length of the cantilever. On the other hand, equivalent mass also depends on the cantilever width, leaving cantilever length and proof mass size as the two parameters with a strong effect on the resonance frequency. Figure 5.14 shows calculated resonance frequencies for varying cantilever length values with and without the 0.5 μm-thick spacer PVDF-TrFE layer. Other parameters used for these calculations are shown in the inset; spacer and active PVDF-TrFE layer thicknesses are 0.5 μm and 2.45 μm, respectively, electrode thicknesses are 0.1 μm, and bulk Si proof mass length is L/4, where L is the cantilever length. The effect of the spacer layer on the resonance frequency was found to be less than 10% for the studied dimension range. An upper limit of 1 kHz was chosen for the multilayer PEHs; therefore, cantilever length range was determined as 800 μm – 2000 μm.

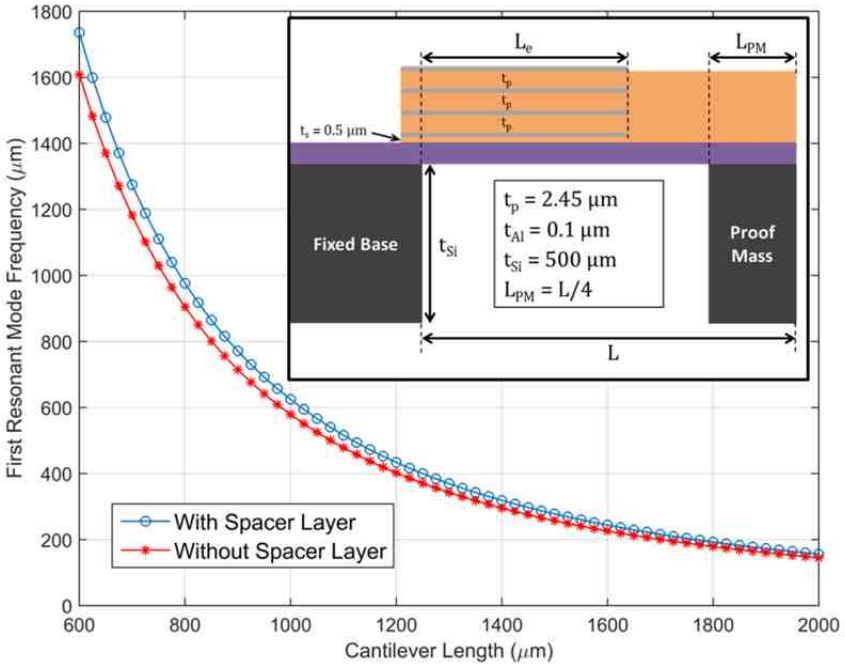


Figure 5.14: Calculated resonance frequency of the cantilever depicted in the inset for different length values. The effect of a 0.5 µm-thick spacer PVDF-TrFE layer on the frequency was found to be less than 10%.

One of the problems encountered occasionally during the tests of the first generation PEHs was disrupted electrode continuity along PVDF-TrFE walls as shown in Figure 5.12. In commercial applications involving multiple electrode layers, such as CMOS IC fabrication, interconnections between different layers are usually fabricated using chemical vapor deposition (CVD) techniques after dedicated isolation layers are deposited and patterned. Although this method provides very reliable connections with high yield, it increases the process complexity. Furthermore, our facilities did not have CVD equipment with metal deposition capabilities. Therefore, a method was necessary to create more reliable connections using PVD techniques, which have relatively low step coverage. Since the continuity problem was a result of the steep walls with almost 90° corners, one possible solution is reducing the slope of PVDF-TrFE edges. This can be

achieved by utilizing grayscale lithography, a technique based on creating a gradually changing ultraviolet (UV) light intensity pattern on the photoresist [121]. The gradual change in the UV intensity is achieved by using mask patterns that are smaller than the resolution of the optical setup that transfers the patterns to the photoresist. Figure 5.15 shows a sample constant-pitch grating pattern that can be used for grayscale lithography. The sample pattern is periodic with period $p = c_i + s_i$, where c_i and s_i denote the length of the dark and clear regions, respectively. If p is close to or smaller than the resolution of the optical system, then a gradually changing UV intensity pattern forms on the photoresist during exposure, instead of the exact shape of the gratings [121]. The UV pattern exposes the photoresist to different depth levels, forming a gradually changing height pattern when developed. The final step is transferring the same pattern to the target layer, which necessitates low etch selectivity between the photoresist and the target layer [122]. This technique is commonly used to fabricate 3D structures on Si for MEMS applications [122, 123].

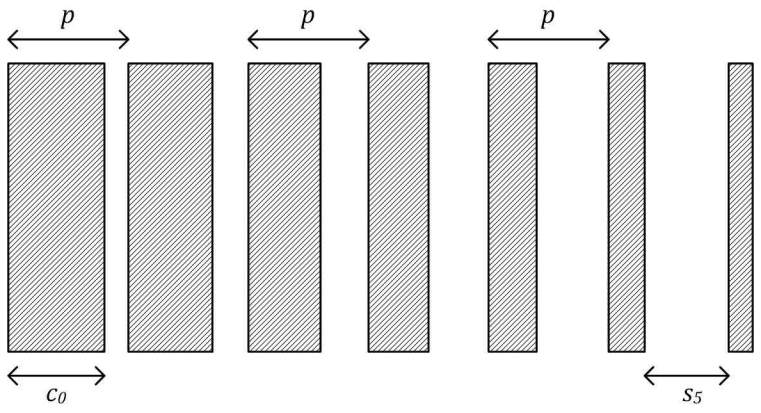
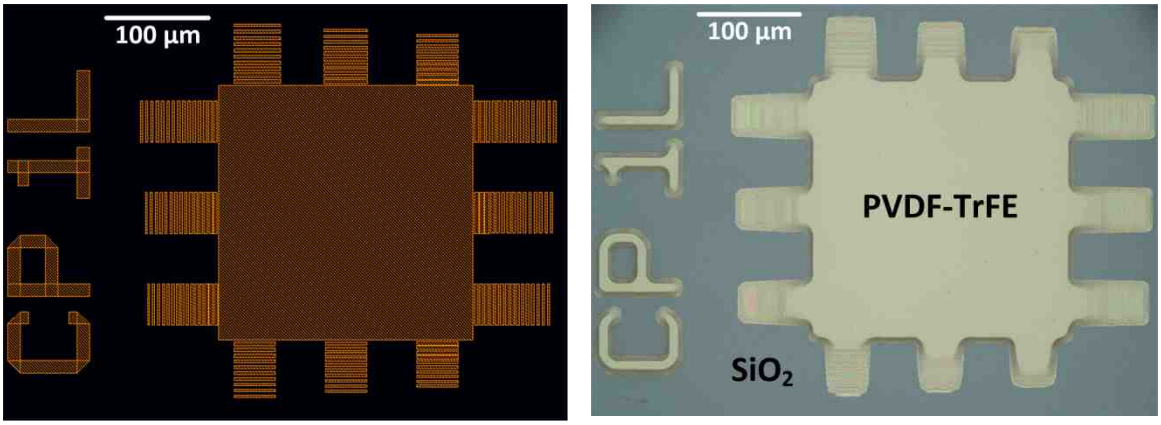


Figure 5.15: Sample constant-pitch grating pattern for grayscale lithography. The structure is periodic with $p = c_i + s_i$, where c_i and s_i denote the dark and clear region lengths, respectively. If the pitch length p is close to the resolution of the optical system, a gradually changing UV pattern can be obtained on the photoresist along the gratings [121].

Grayscale lithography is typically performed using projection steppers, which scale down the patterns on the mask while projecting them on the wafer [121, 122]. The scaling operation relaxes the resolution requirements for the mask; a mask with 2 μm pitch gratings would be projected on the wafer with 0.4 μm pitch size in a stepper with 5:1 ratio. However, since our facilities have only contact lithography equipment, a method had to be developed accordingly. Contact aligners transfer the mask patterns to the wafers with 1:1 ratio; therefore, achieving the same pattern with the previous example would require 0.4 μm pitch gratings on the mask. Such high resolutions are extremely difficult to obtain and way beyond the capabilities of the mask makers in our facilities. As a solution to this problem, the effective resolution of the contact aligner was reduced by proximity lithography, i.e., by exposing the wafers through a gap instead of close contact with the mask. This method has the obvious disadvantage of reduced lithography resolution all over the wafer. Nevertheless, this does not constitute a problem as long as mask design is done with sufficient margins; minimum feature size on the PVDF-TrFE layers in the first generation PEHs was on the order of tens of micrometers.

Before the actual mask design for grayscale lithography, experiments were run to discover the capabilities of the mask maker and to optimize the proximity lithography parameters. Minimum feature size that can be consistently written by the mask maker was found as 1.4 μm and 2.2 μm when drawn parallel and perpendicular to the raster direction, respectively. A test mask was then printed with different grating patterns for grayscale lithography experiments, which were run on SiO_2 coated wafers with 2 – 3 μm-thick PVDF-TrFE films. During the experiments, effect of different photoresist types, exposure doses and mask gaps were investigated. It was found that the photoresist

thickness should be close to PVDF-TrFE thickness for best results. Figure 5.16 (a) shows a sample pattern on the designed test mask. This pattern consists of a 250 µm × 250 µm square surrounded with constant-pitch gratings with different lengths and number of levels. Figure 5.16 (b) shows the microscope image of the corresponding PVDF-TrFE pattern after etching in an O_2 based RIE. This pattern was obtained by coating AZ1518 positive photoresist at 3000 rpm for 60 seconds, exposing it with a UV dose of 40 mW/cm^2 with the gap value set to 100 µm. As seen in the image, all grating patterns created gradually rising steps and resolution loss is less than 5 µm. Therefore, the same recipe was used for the fabrication of the second generation PEHs.



(a) **(b)**

Figure 5.16: (a) Sample mask pattern designed for grayscale lithography experiments. All gratings are constant-pitch with different lengths and levels. (b) PVDF-TrFE thin film patterned using the test mask. All gratings on the test structure gave acceptable results.

Figure 5.17 shows the fabrication process flow of the multilayer devices. The process started with patterning the SiN_x/SiO_2 layers using a CF_4/O_2 based RIE process. Then, the spacer PVDF-TrFE layer was coated in three spin coating steps with 1 hour thermal annealing periods at 140 °C in between. For this layer, an MEK solution with 2% PVDF-TrFE weight ratio was spun at 5000 rpm for 60 seconds in all three steps. The

spacer layer was patterned using the determined grayscale lithography parameters. Etching was done using the same O_2 based RIE recipe, and the average thickness of the layer was measured as 0.55 μm. The first electrode layer was coated by sputtering after patterning the spacer layer. The electrode structure for the multilayer PEHs was determined as Ti/Al/Ti, in order to have the same metal-polymer interface in all layers and to protect the Al layer from being exposed to photoresist developer during lithography. Target thicknesses for the Ti and Al layers were set as 25 nm and 70 nm, respectively, giving a total thickness of 120 nm. Electrode layers were patterned using a (7:1) buffered HF (BHF) solution diluted with water by (1:60). Then, first active PVDF-TrFE layer was coated in four spin coating steps; first three from an 8% weight ratio solution and the final step from a 2% solution. The wafer was annealed in a vacuum oven at 140 °C for 1 hour between spin coating steps and for 2 hours after the final step. Patterning of the active layer was also done using the same grayscale lithography parameters. The same electrode-polymer deposition and patterning processes were repeated to create 3 active PVDF-TrFE layers sandwiched between 4 electrode layers. Electrode masks were designed to have only two terminals for the PEH; one connected to first and third electrodes, and the other connected to second and fourth electrodes, which forms a parallel connection between the 3 capacitors. After the final electrode layer, Ti/Au bonding pads were formed via a lift-off process. Then, a passivation layer was formed to provide electrical isolation and mechanical protection by coating and patterning a 300 nm-thick PVDF-TrFE layer, which finalized the front side process. Proof mass formation and cantilever suspension was realized with the 2-step process used for the first generation PEHs, where the bulk etch was mostly done with DRIE and final

release was done with gaseous XeF_2 etch after front side is cleaned in methanol [70]. It should be noted that although the process includes 12 lithography steps, only 7 different masks were used; spacer and active PVDF-TrFE layers were patterned using the same mask, and 4 electrode layers were patterned using 2 masks.

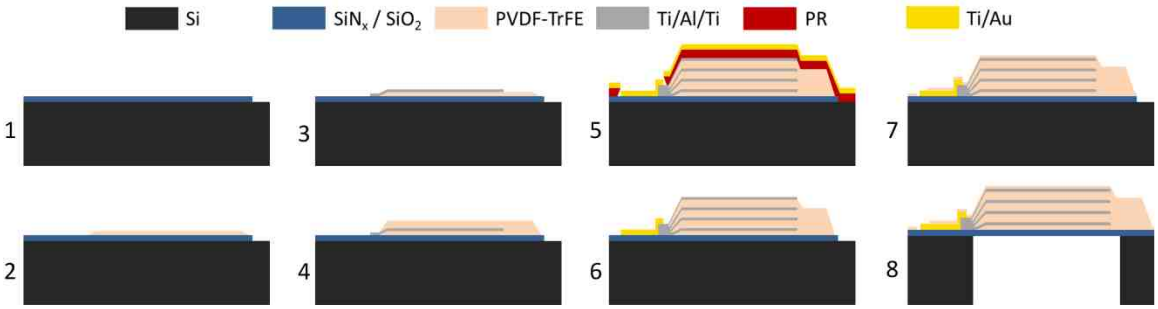
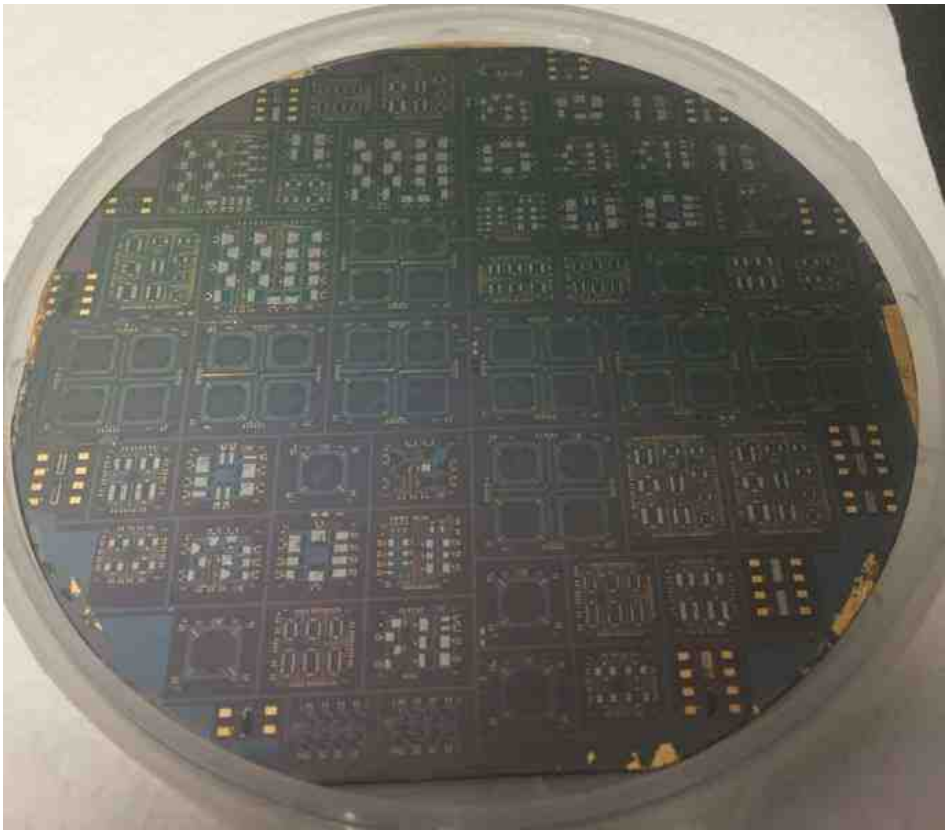
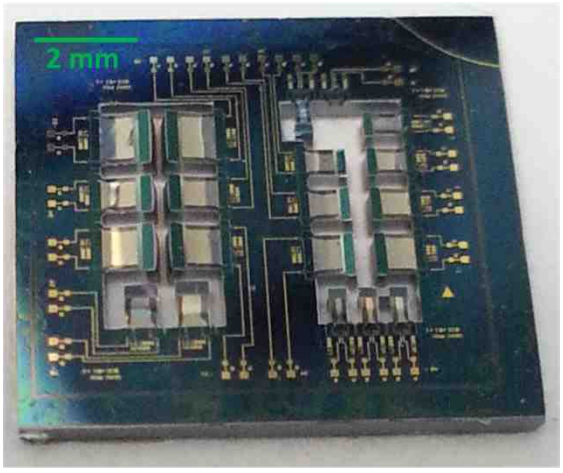


Figure 5.17: Process flow of the multilayer PEHs: (1) Patterning SiN_x/SiO_2 layer with RIE (2) Spacer PVDF-TrFE via spin coating and patterning with RIE (3) Ti/Al/Ti electrodes via sputtering and wet etch (4) Active PVDF-TrFE via spin coating and RIE (5) Ti/Au on top of patterned photoresist via sputtering (6) Bonding pads via lift-off (7) Passivation PVDF-TrFE via spin coating and patterning with RIE (8) Proof mass formation and cantilever suspension with DRIE and XeF_2 etch. Steps (3) and (4) were repeated 3 and 2 more times, respectively, to form 3 active PVDF-TrFE layers sandwiched between 4 electrode layers.

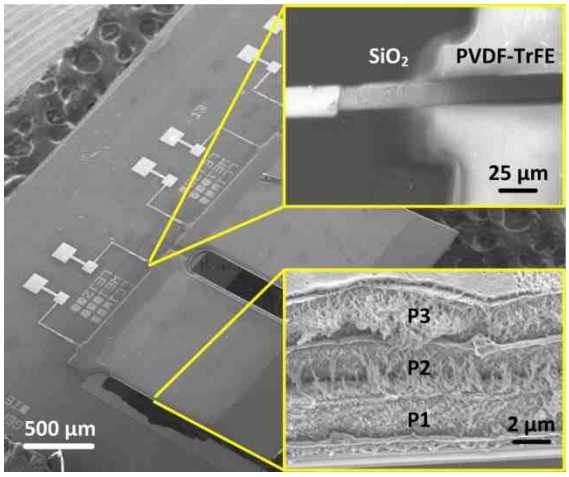
Using the described process, cantilevers with various dimensions were fabricated; length values varied from 800 µm to 2000 µm, and the width values varied from 300 µm to 2000 µm. Proof masses were drawn to have the same width and ¼ length as the cantilevers. Figure 5.18 (a) shows the photograph of the 4" wafer with the multilayer PEHs after front side fabrication. Figure 5.18 (b) shows a die with 20 suspended cantilevers, 12 of them 800 µm-long and the remaining 8 are 1000 µm-long. The total area of the die is 1 cm^2. Figure 5.18 (c) shows SEM images taken from fabricated prototypes; the inset at the top right corner shows the smooth electrode connection over a slanted wall through a step height of approximately 8 µm, and the inset at the bottom right corner shows a close-up view of the multiple PVDF-TrFE layers.



(a)



(b)



(c)

Figure 5.18: (a) Photograph of the 4" wafer with multilayer PEHs before backside process. (b) Photograph of a die with 800 µm-long and 1000 µm-long cantilevers. The 1 cm^2 die includes 20 cantilevers. (c) SEM image of a prototype with 1 mm-wide cantilevers. The inset at the top right corner shows the smooth electrode connection over a slanted wall through a step height of approximately 8 µm. The inset at the bottom right corner shows a closer view of the multiple PVDF-TrFE/electrode layers.

Fabricated multilayer PEH prototypes were wire bonded to standard IC packages for experiments. Samples were poled at room temperature using an electric field strength of 100 V/μm prior to mechanical tests, which were performed using an electrodynamic shaker (Modal Shop K2007E01). Figure 5.19 shows the photograph of the test setup used to characterize the electromechanical energy conversion performance of the PEHs. The setup consisted of a function generator to drive the electrodynamic shaker at different amplitude and frequencies, an accelerometer and its signal conditioner to measure the input vibration amplitudes, a breadboard to connect different electrical loads, and an oscilloscope to observe and record the accelerometer and PEH outputs.

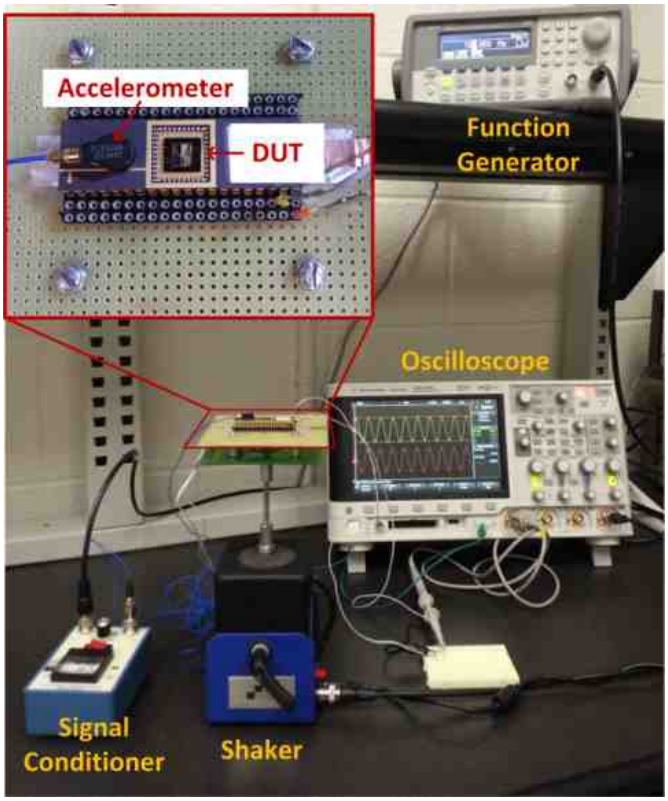
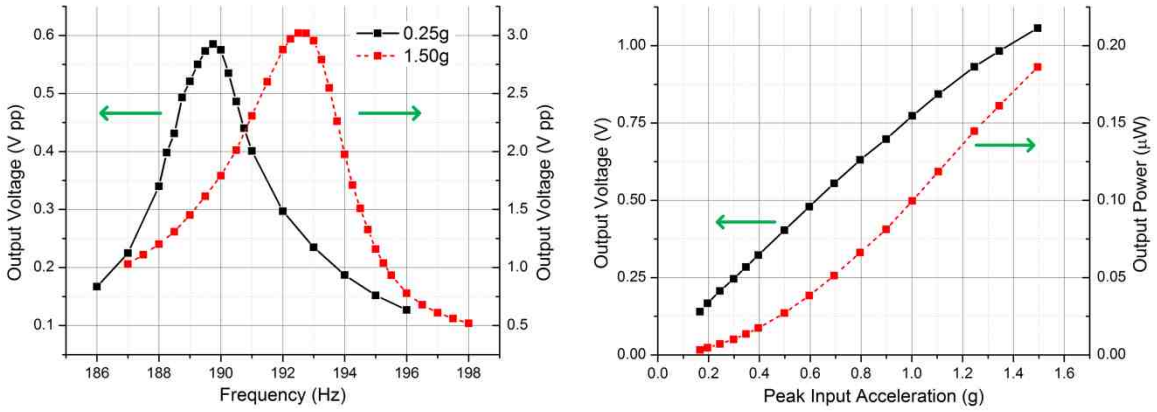


Figure 5.19: Photograph of the test setup used for the mechanical tests of the multilayer PEHs. The shaker was driven with sine waves of different amplitude and frequencies using the function generator to create mechanical vibrations. Both the input acceleration, measured directly from the IC package with an accelerometer, and PEH output were observed and recorded using the oscilloscope.

Measurements from each device were repeated for input acceleration and frequencies as well as different resistive loads. Figure 5.20 shows experimental results obtained from an 1800 μm × 2000 μm prototype. Frequency responses of the PEH under 0.25g and 1.5g peak acceleration values are given in Figure 5.20 (a). Peak-to-peak output voltages were measured as 0.59 V at 189.7 Hz for 0.25g and 3.02 V at 192.5 Hz at 1.5g. Increasing resonance frequency at higher input accelerations is an expected result and can be attributed to the nonlinear stiffness characteristics of cantilevers at large deformations [81]. Mechanical Q factors were estimated from the measured voltages as 74.4 and 61.1 for 0.25g and 1.5g, respectively. The reduction in the Q factor implies that the damping factor increases at higher speeds, again a typical behavior for most mechanical systems. Figure 5.20 (b) illustrates the effects of these nonlinear effects on the output voltage and power as measured on an optimal resistive load of 3 MΩ. Deviation from the linear response reached 5%, 10%, and 25% at 0.6 g, 1.1 g, and 1.5 g peak input acceleration values. Considering that the Q factor at 0.25 g was found to be 22% higher than the Q factor at 1.5 g, it can be concluded that the nonlinearity in the electrical output is due to the mechanical response; piezoelectric response is linear at the encountered strain levels.



(a) **(b)**

Figure 5.20: Experimental results obtained from an 1800 μm × 2000 μm multilayer prototype. (a) Frequency response under 0.25g and 1.50g input acceleration values. (b) Output voltage and maximum power output on an optimal resistive load for different input acceleration values.

Measured electrical outputs were also compared to theoretical values calculated using the analytical formulas presented in Section 2.3.1. For this purpose, average planar stresses T_1 and T_2 were calculated using equations (2.32), (2.34), and (2.35) for zero-stress and zero-strain cases along cantilever width axis. Then, corresponding charge and voltage values were calculated using ideal parallel-plate capacitor assumption. Piezoelectric charge and voltages for zero-stress and zero strain cases can be calculated

$$Q_{free} = d_{31} \cdot T_{1,free} \cdot A \tag{5.1}$$

$$V_{free} = \frac{Q_{free}}{C_p} = \frac{d_{31} \cdot T_{1,free} \cdot t_p}{\varepsilon_{33}} \tag{5.2}$$

$$Q_{clamped} = \left(d_{31} \cdot T_{1,clamped} + d_{32} \cdot T_{2,clamped}\right) \cdot A \tag{5.3}$$

$$V_{clamped} = \frac{Q_{clamped}}{C_p} = \frac{\left(d_{31} \cdot T_{1,clamped} + d_{32} \cdot T_{2,clamped}\right) \cdot t_p}{\varepsilon_{33}} \tag{5.4}$$

where A is the electrode area and ε_{33} is the permittivity of PVDF-TrFE along its polarization axis. Placing the planar stress values as given in equations (2.32), (2.34), and

(2.35) into equations (5.2) and (5.4), open circuit voltages can be written in terms of average strain as

$$V_{free} = \frac{nd_{31}t_p}{\varepsilon_{33}} \cdot \left(c_{11} - c_{12}\frac{c_{12}c_{33} - c_{13}c_{23}}{c_{22}c_{33} - c_{23}^2} - c_{13}\frac{c_{13}c_{22} - c_{12}c_{23}}{c_{22}c_{33} - c_{23}^2} \right) \cdot S_{1,avg} \quad (5.5)$$

$$V_{clamped} = \frac{nt_p}{\varepsilon_{33}} \cdot \left(d_{31} \cdot \left(c_{11} - c_{13}\frac{c_{13}}{c_{33}} \right) + d_{32} \cdot \left(c_{21} - c_{23}\frac{c_{13}}{c_{33}} \right) \right) \cdot S_{1,avg} \quad (5.6)$$

where n is the number of active piezoelectric layers and t_p denotes the thickness of each layer. It can be seen from equation (2.26) that calculating the average strain necessitates neutral axis location and tip displacement data, which could not be measured directly. Instead, neutral axis location was calculated using measured layer thicknesses and average elastic stiffness values taken from literature, and tip displacement was estimated from the measured input acceleration and calculated mechanical Q factor. In highly underdamped systems driven at resonance, input is amplified by a factor approximately equal to Q; therefore, tip displacement was calculated using the formula

$$v_{tip} = Q \cdot v_{base} = Q\frac{a_{base}}{(2\pi f_n)^2} \quad (5.7)$$

where v_{base} and a_{base} are the displacement and acceleration of the cantilever base, respectively, and f_n is the resonance frequency. Piezoelectric and elastic coefficients of the polymer film were taken from a comprehensive characterization study on drawn PVDF-TrFE with 75/25 molar ratio [77]. Figure 5.21 shows the comparison of theoretical and experimental values for the same 1800 μm-long PEH. It should be noted that the theoretical calculations include uncertainties due to material properties; therefore, they have a certain error margin of their own. Nevertheless, it can be seen that the experimental values are approximately at the middle of the range defined by the two

extreme cases. Another important observation is the relation between the output voltage and average strain, which shows a linear piezoelectric response up to average strain levels as high as 0.15%.

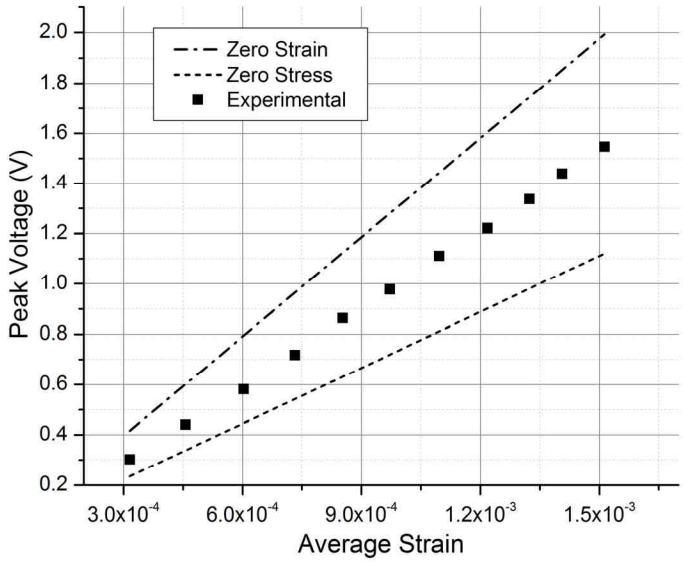


Figure 5.21: Theoretical and experimental values for the open circuit output voltage of the 1800 µm × 2000 µm PEH. Measured voltages increase linearly with average strain and they fit around the middle of the range defined by the two extreme cases.

Same measurements were repeated for prototypes with different dimensions. Figure 5.22 shows a summary of these measurement results. In the plot, *x* and *y* axes show the cantilever length and resonance frequencies, respectively. Each asterisk on the plot denotes measurement results from a PEH prototype, while the dashed line shows the resonance frequency values calculated using measured layer thicknesses, which shows good agreement with experimental values. Normalized area power density (NAPD) values of some devices, which are calculated by dividing the power output per unit area by the square of the input acceleration, are also listed on the plot.

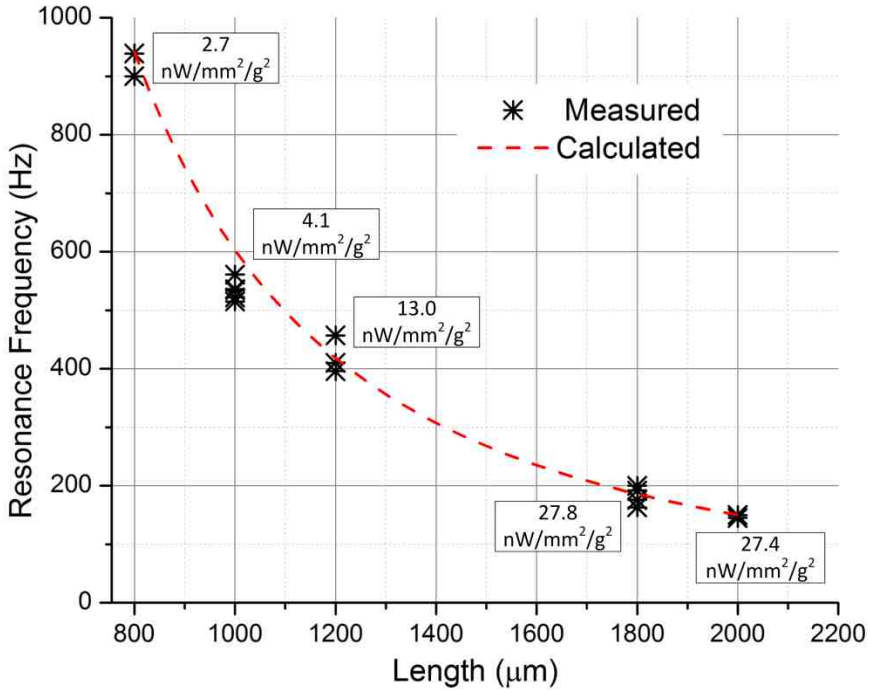


Figure 5.22: Summary of the measurement results obtained from cantilevers with various dimensions.

NAPD is an important metric for energy harvesters since it directly dictates limits on the maximum power output or minimum device area. However, it is not sufficient as a figure of merit to compare the performance of different PEHs, since it does not take some other important factors such operation bandwidth or fabrication complexity into account. Furthermore, NAPD calculation does not completely remove the dependence on frequency and device volume [124]. A figure of merit that eliminates these dependencies and includes the operation bandwidth was proposed by Mitcheson et al., with the name bandwidth figure of merit (FOM_{BW}) [124]. Table 5.1 presents a comparison of fully-microfabricated cantilever type PEHs reported in the literature. The table lists the piezoelectric material, structural layer, device length and volume, and results of energy harvesting experiments for each study. The volume listed in the table includes only the

cantilever beam and proof mass. Half power bandwidth values were approximated from plots if they are not explicitly reported. NAPD values were calculated for all devices, whereas FOM_{BW} values could not be calculated for some of them since their bandwidth data is not reported. It can be seen from the table that the volume of the PVDF-TrFE based PEHs reported in this work are among the smallest, and the devices can achieve resonance frequencies lower than 200 Hz with cantilever lengths below 2 mm. Low NAPD values of the devices can be attributed to the lower electromechanical coupling factor and mechanical Q factor of PVDF-TrFE compared to the other materials. Nevertheless, lower mechanical Q factor translates into a wider bandwidth, and as a result, FOM_{BW} values of the PVDF-TrFE based PEHs are comparable to AlN and ZnO based devices. When considered together with other advantages such as high strain accommodation capability and simple fabrication process, these results show that PVDF-TrFE can be a promising material for CMOS-compatible MEMS scale PEHs.

Table 5.1: Comparison of fully-microfabricated cantilever type PEHs.

Ref.	Year	Piezo Mat.	Str. Layer	L (mm)	Vol (mm^3)	a (g)	f (Hz)	P_{out} (μW)	BW[1] (Hz)	NAPD[2] ($\mu W/mm^2/g^2$)	FOM_{BW}[3] [124]
[37]	2005	Sol-gel PZT	Thin Films	0.26	$4.4x10^{-5}$	10.9	13.9k	1.0	N/A	0.19	N/A
[40]	2008	Sol-gel PZT	Thinned Si	4.8	0.65	2.0	461	2.15	1.4	0.28	$1.01x10^{-4}$
[51]	2008	AlN	SoI	1.2	0.25	0.2	1.58k	0.01	1.8	0.26	$1.29x10^{-6}$
[42]	2009	Sol-gel PZT	SoI	1.2	0.33	0.2	877	0.018	6	0.47	$2.51x10^{-5}$
[44]	2009	Aerosol PZT	SoI	3.0	0.43	1.0	256	1.13	N/A	0.25	N/A
[53]	2010	AlN	SoI	8.2	24.5	1.75	324	85.0	3	0.48	$2.12x10^{-4}$
[45]	2011	Bulk PZT	SoI	7.0	19.7	1.5	415	160.8	33.3	1.46	$3.92x10^{-3}$
[47]	2011	Epi. PZT	Thinned Si	2.5	0.15	1.0	2.3k	13.0	2	13.0	$1.67x10^{-4}$
[49]	2012	AlN	SoI	3.5	1.35	0.2	212	0.59	0.25	2.63	$5.59x10^{-5}$
[57]	2015	ZnO	Thinned Si	2.0	0.8	1.0	1.3k	1.25	3	0.125	$3.49x10^{-6}$
[125]	2016	KNN	SoI	5.0	1.63	1.0	132	3.62	N/A	0.724	N/A
This Work	2017	PVDF-TrFE	Thin Films	2.0	0.19	0.28	149	0.003	2.0	0.027	$1.87x10^{-5}$
				1.8	0.51	0.25	192	0.008	2.5	0.033	$1.22x10^{-5}$
				1.2	0.24	0.3	400	0.002	4.8	0.013	$7.74x10^{-6}$

[1] BW: Half power bandwidth
[2] NAPD: Normalized area power density
[3] FOM_{BW}: Bandwidth figure of merit

CHAPTER 6: INTEGRATION WITH ELECTRONICS

The ultimate goal of vibration energy harvesting systems is transferring the ambient mechanical energy to their electrical loads. The efficiency of this process depends not only on the mechanical design of the harvester, but also on its electrical interface. Power output levels of PEHs are typically reported for purely resistive loads. Figure 6.1 shows a simple weakly-coupled PEH model with a purely resistive load. It is readily seen from the schematic that the power transferred to the load depends on its resistance. Maximum power transfer occurs when $R_L = 1/(\omega C_p)$, where ω is the operating frequency.

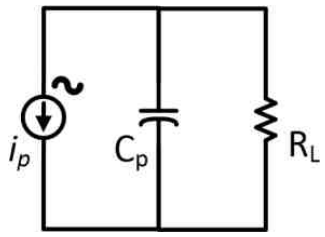


Figure 6.1: Weakly coupled PEH model with purely resistive load.

The main disadvantage of a resistive load is the instantaneous dissipation of the harvested power; a resistor cannot store energy for later use. Therefore, a more practical approach is converting the AC output of the PEHs into DC, which can be stored in capacitors or batteries to be used when needed. Figure 6.2 shows a weakly coupled PEH model with a 4-diode full wave rectifier type AC-DC converter load, which can be used for this purpose.

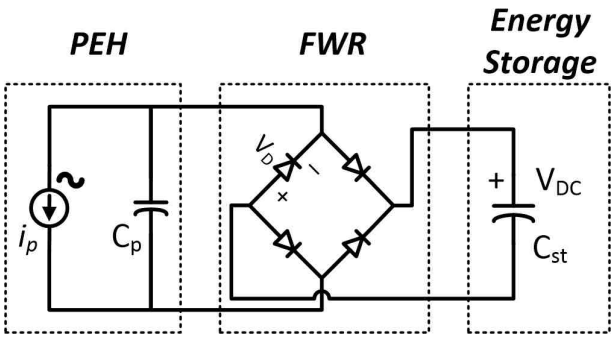


Figure 6.2: Weakly coupled PEH model with a 4-diode full wave rectifier type AC-DC converter load.

The DC level of the output can be assumed constant in the circuit depicted in Figure 6.2 in case of a battery or a very large storage capacitor. It can be shown that the power transferred to the load depends on this DC level, and it is maximized at

$$V_{DC,opt} = \frac{i_p}{2\omega C_p} - V_D = \frac{V_{OC}}{2} - V_D \tag{6.1}$$

where ω is the angular frequency of operation, V_{OC} is the peak open circuit voltage of the PEH, and V_D is the diode forward voltage drop [74]. This equation indicates that unlike the resistive load case, optimal electrical load varies with input excitation level when a rectifier is used [88]. In order to track this optimal point, utilizing adaptive DC-DC converters between the full wave rectifier and energy storage element has been proposed by Ottman et al. [88, 126]. However, control circuits of the DC-DC converters proposed in these studies require milliwatt-level powers, which is much higher than the output of typical MEMS scale PEHs. Furthermore, power output is only 64% of the purely resistive load case, even at optimal DC output voltage and negligible rectifier losses [74]. Rectifier losses occur on conducting diodes due to voltage forward voltage drop; and therefore, they can reach significant levels in small scale devices with low output voltages, where V_D is comparable to V_{OC}. To exemplify, the diodes would dissipate 64% of the PEH

output power when $V_{OC} = 5V_D$, yielding only 23% of the power obtainable with a resistive load [74]. Consequently, more efficient electrical interfaces are crucial especially for MEMS scale PEHs with DC loads.

Modifying the resistive load or the DC output level can be classified as passive power optimization methods; since the electrical load consists of only passive elements. With these loads, output voltage is simply determined by the PEH current, which depends solely on the mechanical input for a given PEH design, and total impedance driven by this current. Therefore, PEH voltage is limited to its open circuit value with passive methods. On the other hand, active control circuits can be used to increase the voltage beyond the open circuit values, leading to higher power outputs. Such active circuits rely on switches triggered at the zero crossings of the PEH current; and therefore, they are commonly referred as synchronous switched circuits. Increased voltage levels also reduce the percentage of rectifier losses for PEHs with DC outputs, which is a significant advantage for small scale PEHs.

In this study, various synchronous switched circuit topologies were examined for their feasibility to be integrated with the fabricated PEH prototypes. The following section briefly presents the theory of synchronous switched circuits and discusses the reasoning behind the chosen architecture. Design details of two different low-power synchronous switched energy harvesting circuits, one completed at transistor level using a 0.6 μm CMOS process and the other one at board level using discrete components, are presented in Section 6.2. Operation of the transistor level design was verified with simulations, whereas the board level design was implemented on a printed circuit board

(PCB) and its proper operation was verified experimentally using fabricated PEH prototypes.

6.1 Synchronous Switched Energy Harvesting Circuits

The main idea behind synchronous switched energy harvesting circuits is to extract the current at higher average voltage levels, leading to higher power outputs [74, 127]. In order to achieve this, electrical load is kept disconnected from the PEH except at the voltage peaking instants, allowing the energy to build up in the PEH capacitor before being transferred to the load [128]. Figure 6.3 (a) shows a block diagram for a synchronous switched energy extraction (SSE) system. The switch between the PEH and the electrical load is controlled by a circuit, which generates narrow pulses at the voltage peaks to close the switch. Figure 6.3 (b) shows the voltage and current waveforms on a PEH with and without an SSE circuit. When the switch is closed, all charge accumulated on the PEH is transferred to the load, after which the switch is opened again. This process increases the peak voltage on the PEH, since the voltage has always the same sign as the generated current. The energy stored in a linear capacitor is proportional to the square of its voltage; therefore, more electrical energy is stored in the PEH and then transferred to the load in every cycle. It has been shown theoretically that this circuit can increase the power output transferred to a DC load by up to 300% compared to a simple rectifier [74].

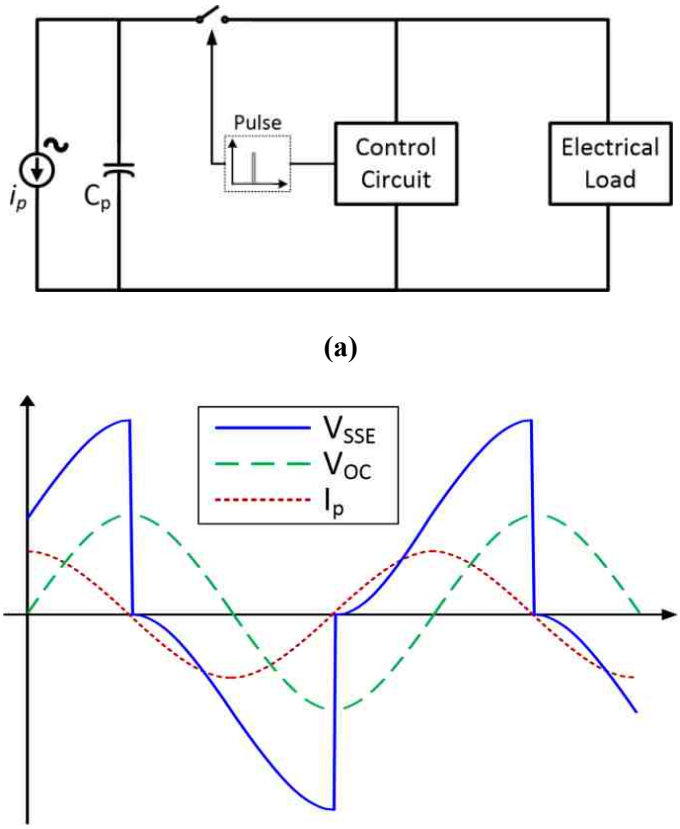
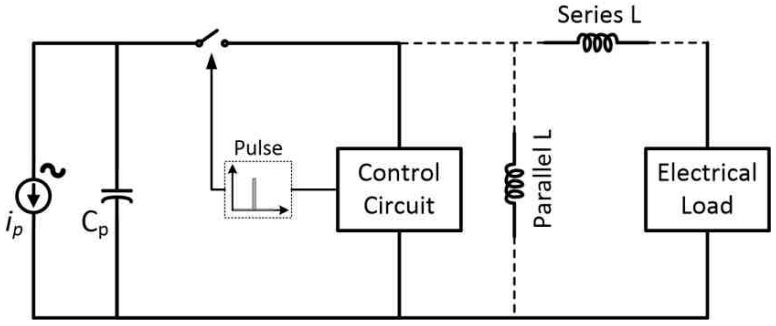


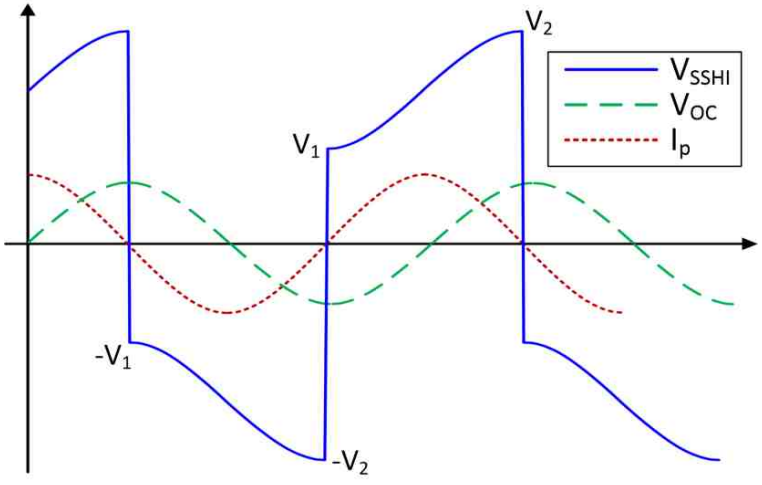
Figure 6.3: (a) Block diagram of an SSE circuit. The control circuit shortly closes the switch at the voltage peaks to transfer the charge to the load. (b) Voltage and current waveforms of a PEH with an SSE interface. Open circuit voltage is also shown for comparison.

Further improvement in the power output can be achieved by inverting the PEH voltage at the peak values instead of simply removing the charge [74]. Piezoelectric voltage polarity can be inverted by connecting an inductor to the PEH momentarily, forming an RLC oscillator. This technique, named synchronized switch harvesting on inductor (SSHI) has first been introduced by Guyomar et al. [72]. Figure 6.4 (a) shows the block diagram of an SSHI circuit, which is very similar to SSE except the presence of an inductor connected either in parallel or in series with the load. Resultant voltage waveform is shown in Figure 6.4 (b) along with the current and open circuit voltage of

the PEH. When the PEH voltage reaches its steady-state peak value, the switch is closed, forming an RLC oscillator circuit. The switch is kept closed until the voltage reaches its peak value at the reverse polarity, which corresponds to one half period of the RLC circuit [72]. After the switch is opened, the current generated by the PEH motion continues driving the voltage. The increase in the voltage amplitude during this period compensates for the losses during the inversion due to the finite *Q*-factor of the RLC network, at which point a steady-state is reached [72].



(a)



(b)

Figure 6.4: (a) Simplified schematic of an SSHI circuit. The inductor can be placed in parallel or in series with the load. (b) Open circuit voltage with and without SSHI. Current generated by the PEH is also shown.

Exact voltage amplitudes in an SSHI circuit with perfect timing and weakly-coupled piezoelectric structure depend on including the type of the inductor connection (series or parallel), Q factor of the RLC network, and electrical load [74]. One of the most important differences between the parallel and series SSHI configurations for rectifier loads is the minimum voltage requirement. Figure 6.5 illustrates the equivalent circuit configurations of (a) parallel and (b) series SSHI with a rectifier connected to the output. In the parallel circuit, the current loop through the inductor does not contain any components except the switch. Therefore, even very small voltages can drive current through the inductor, starting the voltage inversion process. On the other hand, the loop has two diodes in the series circuit, requiring a minimum voltage of $2V_D$ to initiate current flow through the inductor. For this reason, parallel SSHI architecture has been chosen for integration with the fabricated CMOS compatible PEH prototypes.

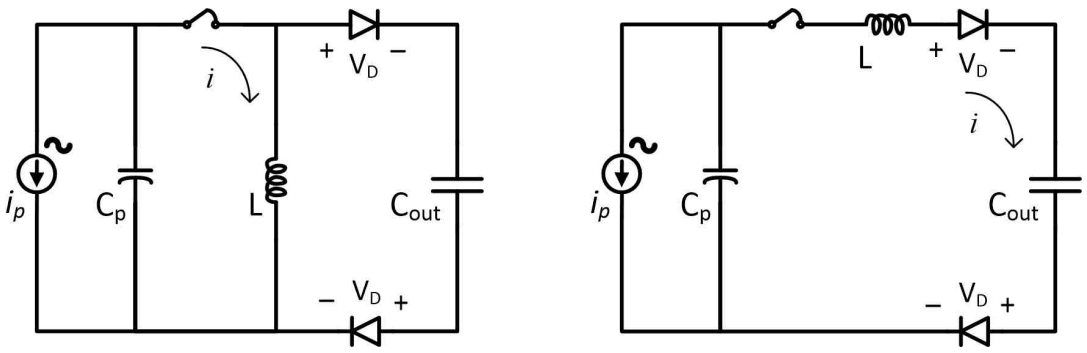


Figure 6.5: Equivalent circuits of (a) parallel and (b) series SSHI with a rectifier type load. Parallel SSHI can drive current onto the inductor at any voltage, whereas the series circuit requires a minimum voltage of $2V_D$ on the capacitor to initiate the current.

Detailed calculations of parallel and series SSHI circuits can be found elsewhere [73, 74, 129, 130] and will not be discussed in this thesis. Nevertheless, it is necessary to present a brief analysis of the parallel SSHI circuit for the sake of completeness. Using

the simplified PEH model for weakly coupled systems and assuming ideal switch timing, the relation between the voltage amplitudes V_1 and V_2 as shown in Figure 6.4 (b) can be calculated as

$$V_1 \cong V_2 \cdot e^{-\pi/2Q} \tag{6.2}$$

where Q is the electrical Q factor of the RLC network [74]. At steady state, generated current drives the voltage amplitude from V_1 to V_2 after the inversion process. Total charge generated during this phase can be calculated from the open circuit voltage of the PEH as $\left(2V_{OC} \cdot C_p\right)$. It should be noted that part of this charge can flow through the load, which is always directly connected to the PEH in parallel SSHI configuration [74]. If this load is a full wave rectifier driving a voltage V_{DC}, and the diodes are modeled as ideal elements with a constant forward voltage drop V_D, PEH voltage must build up to $(V_{DC} + 2V_D)$ to turn on the diodes. After this point, the voltage is clamped and all the generated current is transferred into the load. The optimal value of V_{DC} and corresponding output power in this case are equal to

$$V_{DC,opt} = \frac{V_{OC}}{1 - e^{-\pi/2Q}} - V_D \tag{6.3}$$

$$P_{max} \cong \left(1 - \frac{\pi}{2Q}\frac{V_D}{V_{OC}}\right)^2 \cdot \frac{2Q}{\pi^2} \cdot \frac{i_p^2}{\omega C_p} = \left(1 - \frac{\pi}{2Q}\frac{V_D}{V_{OC}}\right)^2 \cdot \frac{8Q}{\pi^2} \cdot P_{max,R} \tag{6.4}$$

where $P_{max,R}$ is the maximum power output for a purely resistive load [74]. This equation shows that the minimum open circuit voltage requirement to operate the rectifier is

$$V_{OC,min} = \frac{\pi}{2Q} \cdot V_D \tag{6.5}$$

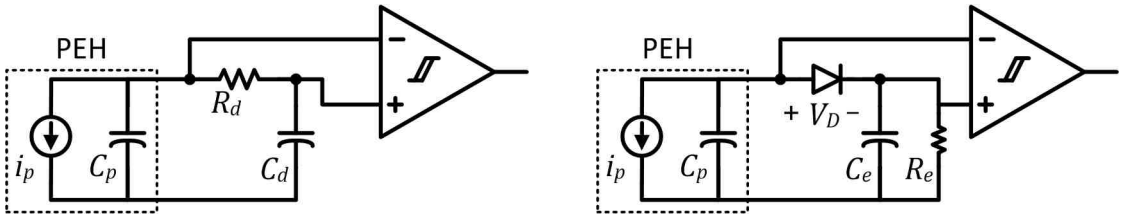
instead of $2V_D$ required in case of standard full wave rectifier or series SSHI interfaces [74]. In addition to relaxing the minimum voltage requirement, a high Q factor also

improves the power output as indicated by Equation (6.4). However, it should be noted that the SSHI interface requires the addition of a control circuit to drive the switch. Consequently, the power dissipated by this control circuit should also be considered while calculating the power gain. Furthermore, power gain is further reduced in practical circuits due to non-idealities such as the delays in the pulse, non-ideal pulse width, and switch charge injection. Therefore, circuit design should be done to minimize the effects of these non-idealities, as described in the following section.

6.2 Low Power SSHI Circuit Design

The function of the control circuit in an SSHI interface is to control the switch timing. Therefore, it must be able to detect the voltage peaks, or equivalently, zero current crossings. Another important requirement, especially for small scale PEHs, is low power dissipation; the power gain provided by the SSHI operation must be higher than the power dissipated by the control circuit.

Voltage peak instant detection is usually performed using comparators; by comparing the input voltage to either with its delayed version [131] or its envelope [132]. Figure 6.6 shows the schematics for (a) delayed signal comparison and (b) envelope comparison for peak detection. The output of the delayed signal comparison circuit toggles at the positive and negative voltage peaks; therefore, it allows the detection of peaks at both polarities. On the other hand, envelope comparison requires two separate circuits to detect the peaks at opposite polarities. More importantly, its output does not toggle until the voltage falls below the peak value at least by diode forward voltage V_D. This delay can be unacceptable for PEHs with low voltage outputs. Therefore, delayed signal comparison method was chosen for this work.



(a) **(b)**

Figure 6.6: Peak instant detection using comparators. The signal can be compared with (a) delayed version of itself, or (b) its envelope. Delayed signal comparison toggles the output at both positive and negative peaks, whereas two separate circuits are required to detect the positive and negative peaks in envelope comparison.

The effective input of the comparator, namely the voltage difference between its positive and negative input terminals, can be calculated as

$$V_{comp,in} = V_p \cdot \frac{-j\omega R_d C_d}{1 + j\omega R_d C_d} \tag{6.6}$$

for a sinusoidal input voltage V_p, if the non-ideal effects due to finite input impedance and input bias currents are neglected. Amplitude and phase of the effective input are then equal to

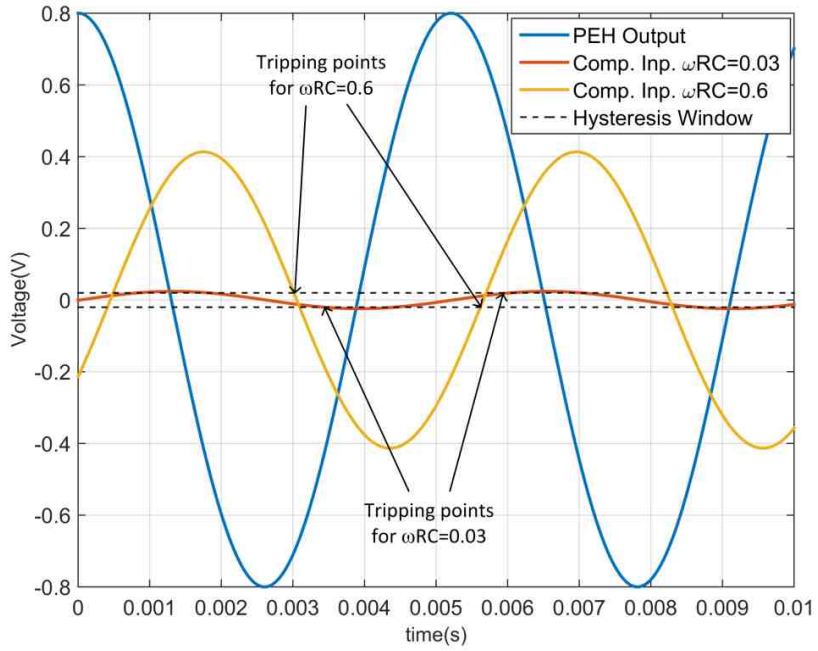
$$\left|V_{comp,in}\right| = V_p \cdot \frac{\omega R_d C_d}{\sqrt{1 + (\omega R_d C_d)^2}} \tag{6.7}$$

$$\angle V_{comp,in} = \varphi_d = -\frac{\pi}{2} - \tan^{-1}(\omega R_d C_d) \tag{6.8}$$

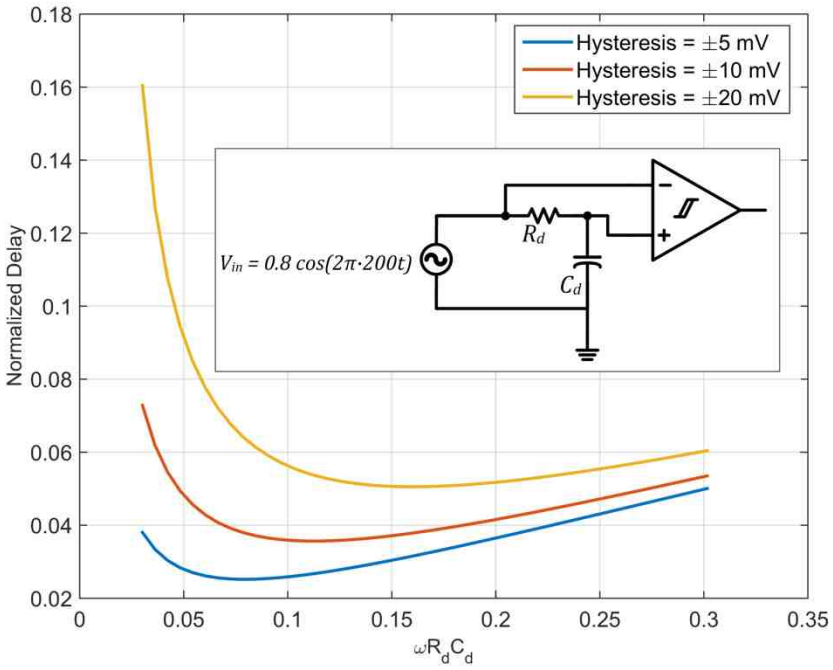
The phase of the effective comparator input determines the error in the output toggling instants; ideally there must be a phase difference of ±π/2 between the PEH output and effective comparator input. Therefore, the term $\omega R_d C_d$ must be minimized for better timing. On the other hand, practical comparators have internal or external hysteresis to provide noise immunity; and therefore there is a minimum effective input amplitude required for proper operation. For $\omega R_d C_d \ll 1$, effective comparator input would be approximately equal to

$$\left|V_{comp,in}\right| \cong V_p \cdot \omega R_d C_d \tag{6.9}$$

Consequently, the values chosen for R_d and C_d determine the delay between actual voltage peak and comparator output toggling instant, and set a threshold for the minimum PEH output voltage required to trigger SSHI operation. The amplitude of the effective comparator input can also affect the delay if it is comparable to the hysteresis window of the comparator. Figure 6.7 (a) shows the PEH output and corresponding effective comparator inputs for two different ωRC values, 0.03 and 0.6. The dashed lines show a hysteresis window of ±20 mV for the comparator; the intersections of these lines and the effective inputs define the output tripping points as labeled on the figure. It can be clearly seen that despite the smaller phase angle, the tripping delay of the circuit with smaller ωRC is worse because of the time required for the input to exceed the hysteresis threshold. These tripping delays depend on the input amplitude and comparator hysteresis window; therefore, there is no single optimal value for the ωRC of the delay circuit. Figure 6.7 (b) shows the calculated tripping delays normalized to waveform period for the circuit depicted in the inset with three different comparator hysteresis windows. Decreasing the hysteresis window size reduces the tripping delays; on the other hand, it makes the control circuit susceptible to noise and high frequency signals generated during switching operations. Therefore, hysteresis window of the comparator should be designed as small as possible without causing false tripping.



(a)



(b)

Figure 6.7: (a) Illustration of the effect of comparator hysteresis on the output tripping delay. The delay of the circuit with ωRC = 0.03 is worse than the one with ωRC = 0.6 due to the ±20 mV hysteresis window. (b) Calculated normalized tripping delays of the circuit given in the inset for different hysteresis windows. Input amplitude also affects the delays; the effect of hysteresis windows decreases at higher input amplitudes.

Voltage peak instants of the PEH can be detected with a certain error margin by using a comparator and a delay circuit as described above. However, this circuit would generate a square wave, whereas SSHI necessitates the switch to be closed only until the PEH voltage reaches its peak at the opposite polarity. Nevertheless, the square wave output can be used in combination with switching circuits that utilize diodes. Figure 6.8 shows an SSHI circuit implemented using a multiplexer switch and two diodes [133]. In this circuit, the switch and comparator output polarity are configured to keep the diodes reverse biased at all times except for the switching instants. When the comparator output changes, a low impedance path is formed and current starts flowing through the inductor. The diode automatically turns off the current when the voltage polarity is flipped, eliminating the need for a carefully adjusted short pulse. However, this circuit suffers from an important drawback for low voltage/current systems. Equivalent resistance of a diode is inversely proportional to its current; and therefore, presence of a series diode on the inductor current path can severely limit the electrical Q factor in case of low currents.

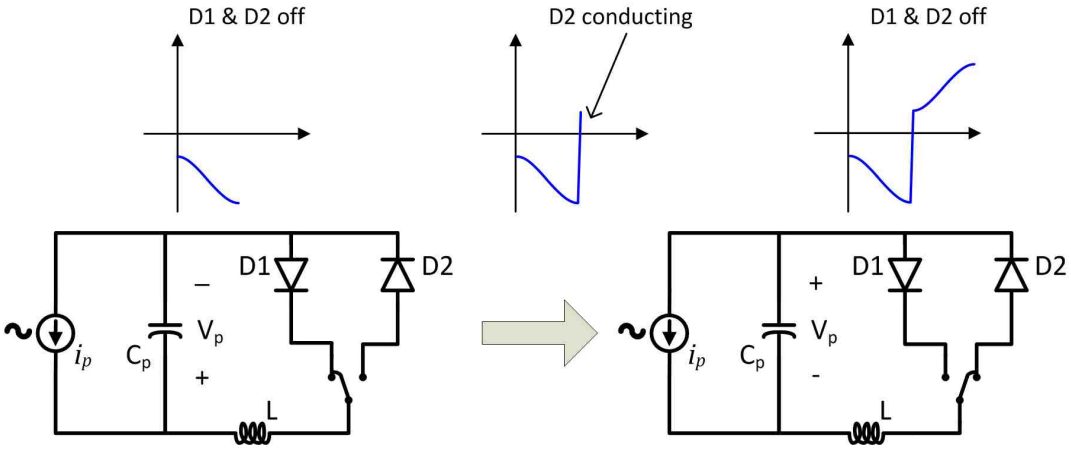


Figure 6.8: SSHI circuit that can be driven by a single peak detecting comparator [133]. Comparator output is connected to the switch such that both diodes reverse-biased at all times except for the switching instants. Once the voltage polarity is flipped, diodes automatically turn off the current.

The other option to drive an SSHI circuit using the output of a peak detecting comparator is generating a pulse from the square wave generated by the comparator. This can be simply achieved by applying the square wave and its delayed version to the inputs of an XOR logic gate. The pulse width is determined by the duration of this delay; and therefore it must be adjusted according to the given capacitance and inductor values. This adjustment can be done during the design phase for a specific PEH. It is also possible to create modular designs where the delay can be adjusted via external control signals or special techniques such as laser trimming for on-chip designs.

After considering the advantage and disadvantages of the different approaches examined so far, power conditioning circuit topology was chosen as a parallel SSHI interface with a single switch driven by short pulses. Figure 6.9 shows the general block diagram of the designed SSHI pulse generator circuit. Two delay networks, $R_{d,1}/C_{d,1}$ and $R_{d,2}/C_{d,2}$, determine the tripping delay and pulse width, respectively. The design of this circuit was completed both at transistor level and board level. Operation of the former was verified with simulations, whereas the board level design was fully implemented and its operation was experimentally verified.

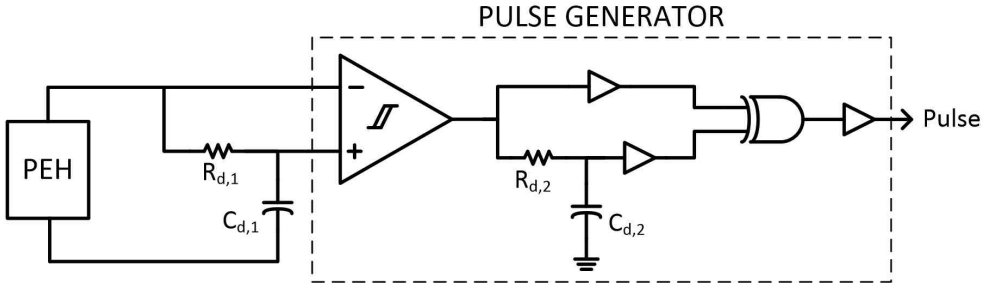


Figure 6.9: Block diagram of the designed SSHI pulse generator circuit. The first delay network determines the pulse delay and minimum PEH voltage required to operate the circuit. The second delay network determines the pulse width.

6.2.1 Transistor Level Design

Fabrication of transistor level circuits is beyond the scope of this dissertation; and therefore, physical implementation and integration of an SSHI circuit with fabricated PEH prototypes were done only at board level. Nevertheless, a transistor level schematic design was completed to provide a basis for potential future CMOS integration. All blocks of a pulse generator circuit and a complementary switch was designed at transistor level in Cadence environment using the open source design kit NCSU CDK v1.6.0.beta, which is based on a 0.6 μm CMOS process. Completed SSHI design was simulated in combination with a weakly coupled PEH model, an AC current source in parallel with a capacitor, using Spectre.

As depicted in Figure 6.9, pulse generator circuit consists of a comparator followed by an RC delay network and some logic gates. The comparator was designed using well-known circuit topologies. Figure 6.10 shows its schematic view, which consists of a supply-independent current source, a decision circuit with positive feedback, and a digital buffer section to improve the transient response of the output. The inverters in the digital section start with minimum size transistors and scale up at every stage in order to minimize the crowbar current due to slow rising gate inputs. Supply lines of the inverters are also separated from the preceding analog blocks in order to be able to reduce the voltage headroom, which decreases both dynamic CMOS power dissipation and crowbar current. Positive feedback was scaled via transistor dimensions to yield a hysteresis window of ±7.5 mV. The dimensions of all transistors in the comparator are listed in Table 6.1.

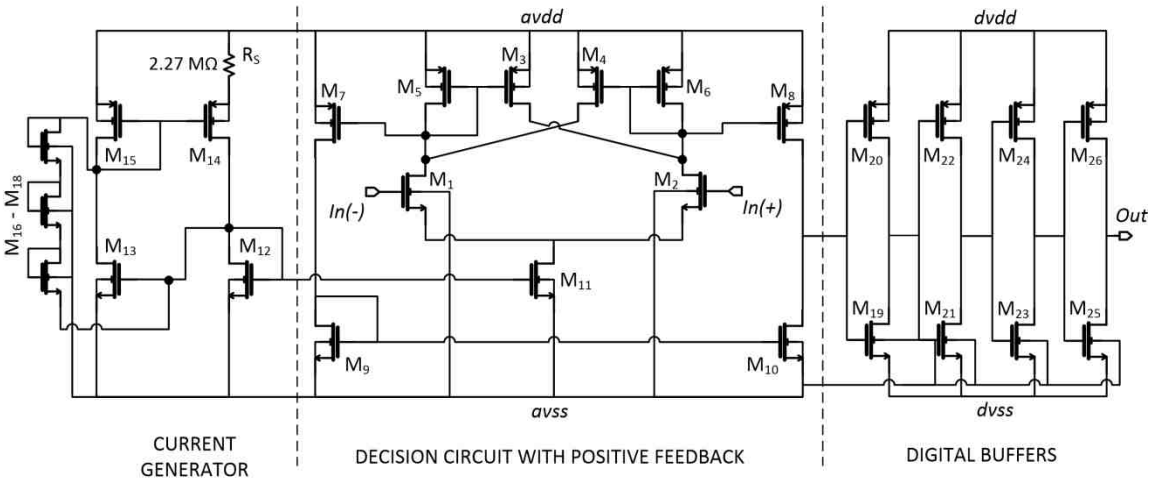


Figure 6.10: Schematic of the comparator, which consists of a supply-independent current generator, a decision circuit with positive feedback, and digital buffers. Digital buffers can be operated from a lower supply to reduce crowbar current and dynamic power dissipation.

Table 6.1: Transistor dimensions of the designed comparator.

	W/L (µm)		W/L (µm)		W/L (µm)
M_1, M_2	32.4/1.95	**M_{12}, M_{13}**	24.0/15.0	**M_{21}**	3.6/0.6
M_3, M_4	22.5/0.9	**M_{14}**	36.0/13.5	**M_{22}**	9.0/0.6
M_5, M_6	36.0/1.2	**M_{15}**	27.0/13.5	**M_{23}**	9.0/0.6
M_7, M_8	7.5/0.9	**M_{16} - M_{18}**	1.5/12.0	**M_{24}**	22.5/0.6
M_9, M_{10}	2.85/0.9	**M_{19}**	1.5/0.6	**M_{25}**	23.1/0.6
M_{11}	21.0/15.0	**M_{20}**	3.6/0.6	**M_{26}**	53.85/0.6

Figure 6.11 shows the results of two different transient simulations of the comparator with the negative input terminal connected to ground. A dual supply scheme was used in these simulations; *avdd* and *dvdd* were connected to the positive supply, *avss* was connected to negative supply, and *dvss* was connected to ground. Average analog and digital currents for a 0.6 pF capacitive load were calculated as 15.4 nA and 0.16 nA at ±0.8 V supplies, and 19.8 nA and 0.32 nA at ±1.5 V supplies, respectively. Corresponding power dissipation values are 24.8 nW and 59.9 nW, which are easily attainable even with MEMS scale PEHs.

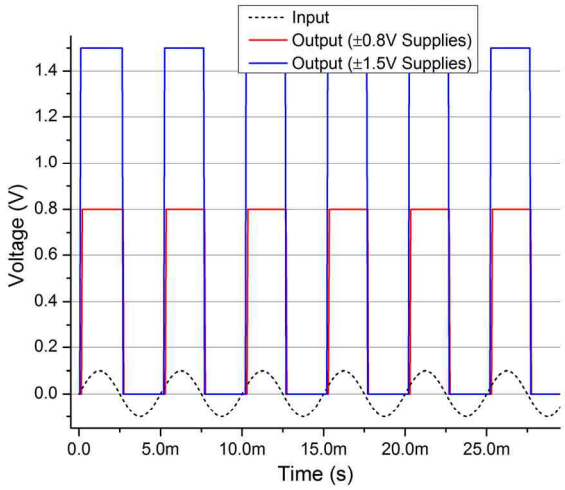
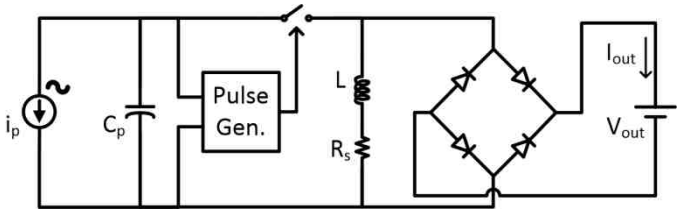


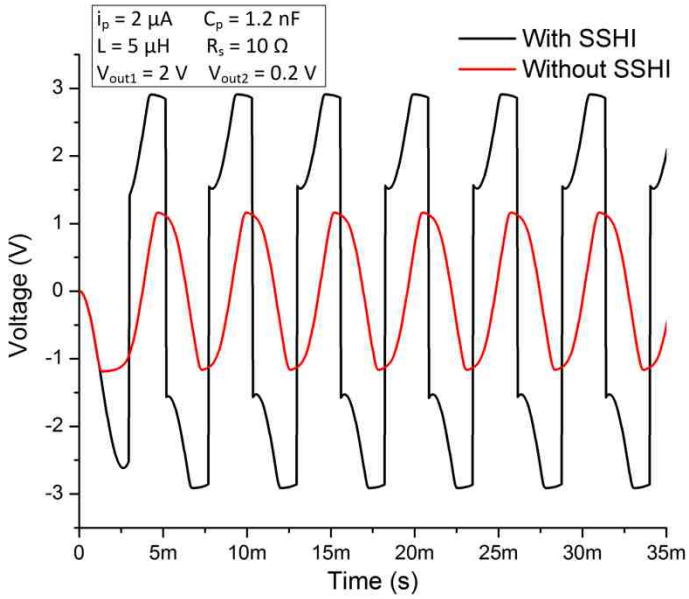
Figure 6.11: Transient simulation results of the comparator with the negative input terminal connected to ground. Analog and digital sections were operated from dual and single supply voltages, respectively.

The logic blocks following the comparator convert its square wave output into narrow pulses triggered at the rising and falling edges. These logic gates were designed using the standard CMOS topology with PMOS type pull-up and NMOS type pull-down networks; therefore, their details will not be presented here. Completed pulse generator circuit was combined with a CMOS switch to create a full SSHI circuit at transistor level. Operation of this transistor level design was verified via simulations in Cadence environment using the schematic shown in Figure 6.12 (a). In this schematic, i_p and C_p are used to model the PEH, L and R_s are used to model an inductor with series resistance, and V_{out} is used to model a battery connected to the output of the rectifier. All other components, including the full wave rectifier, were designed at transistor level. Figure 6.12 (b) shows the results of a transient simulation run using identical PEH models with and without SSHI circuits. Circuit parameters used in the simulation are listed on the figure. It is worth pointing out that optimal output voltage values were used in both cases, 2.0 V and 0.2 V, resulting in average power outputs of 1.14 μW and 46 nW, with and

without the SSHI, respectively. Power dissipated by the SSHI circuit in the same simulation was calculated as 220 nW, yielding a net power output of 0.92 µW.



(a)



(b)

Figure 6.12: (a) Setup used to simulate the designed SSHI circuit. (b) Transient simulation results showing the voltage waveforms with and without SSHI. Both cases were simulated with optimal DC values at the output, 2.0 V and 0.2 V, respectively.

6.2.2 Board Level Design

Simulations of the transistor level design verified the proper operation of the pulse generator topology depicted in Figure 6.9. Since this is a simple topology consisting of a comparator followed by standard logic gates and a switch, no new simulations were conducted for the board level design and a circuit with the same signal flow was designed

using discrete components. Figure 6.13 shows the schematic of the designed board level SSHI circuit. In this design, comparator is followed by a level translator to reduce the voltage headroom and hence, power dissipation of subsequent digitals. Voltage level is then increased again using another level translator and buffered before driving the switch. Part numbers of the selected components, which were mainly chosen for their low power consumption, are also shown on the figure. In order to ensure proper operation of the circuit with different voltage supply configurations, two options were considered for the comparator and the switch ICs. Furthermore, full wave rectifiers with both standard and Schottky diodes were considered for the experiments. PCB design was done in a modular way that enables the implementation of these different options.

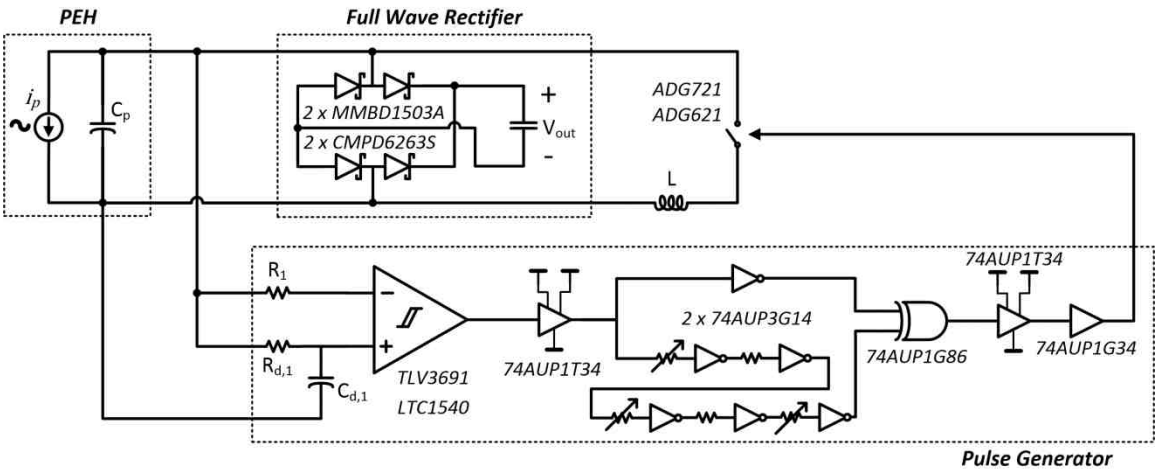
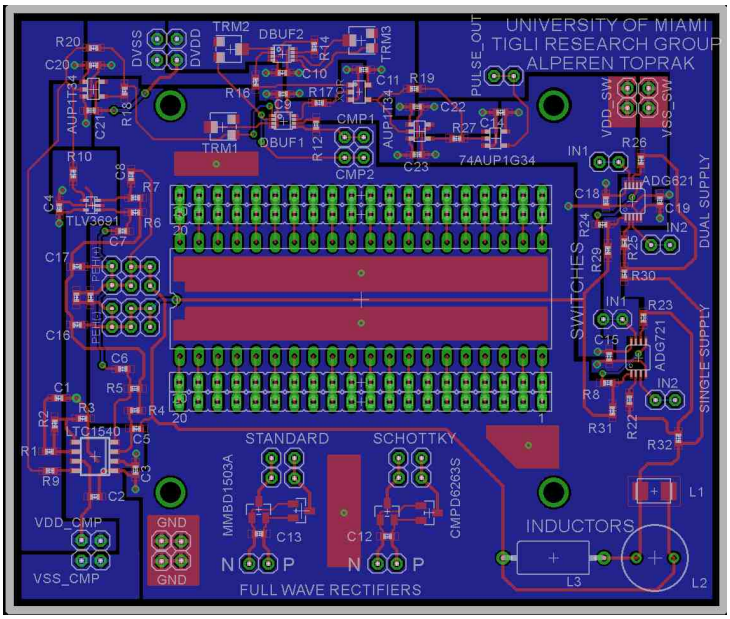


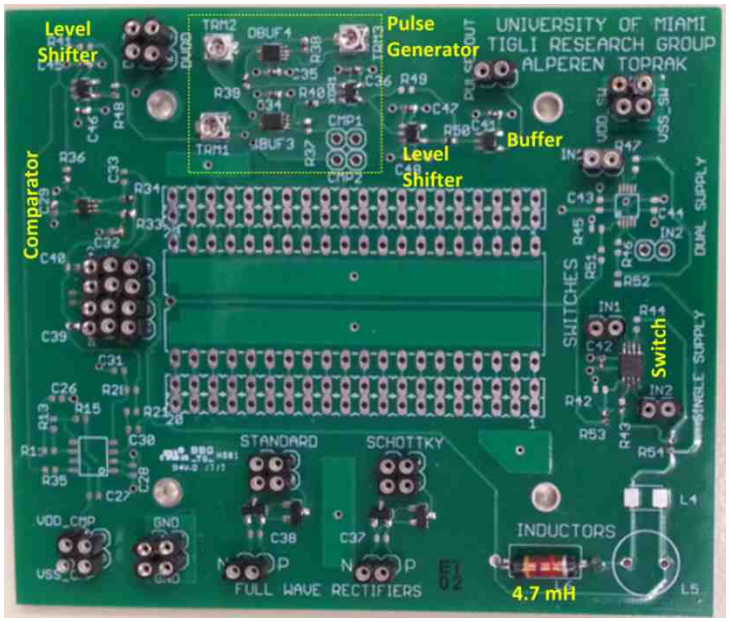
Figure 6.13: Schematic of the SSHI circuit implemented at board level. Part numbers of the selected components are also shown in the figure. More than one option was considered for some components, and the design was done to accommodate these different options.

Two different PCBs were designed with the given circuit configuration; one for DIP40 and the other for PLCC84 type IC packages, which were used to wire bond the fabricated prototypes. Figure 6.14 (a) shows the layout of the 2-layer PCB designed for DIP40 type packages, and Figure 6.14 (b) shows the photograph of the same design

populated with TLV3691 comparator, voltage level shifters, buffers, and ADG721 switch. A through-hole 4.7 mH inductor was connected for the voltage inversion. Both standard and Schottky full wave rectifiers were also populated.



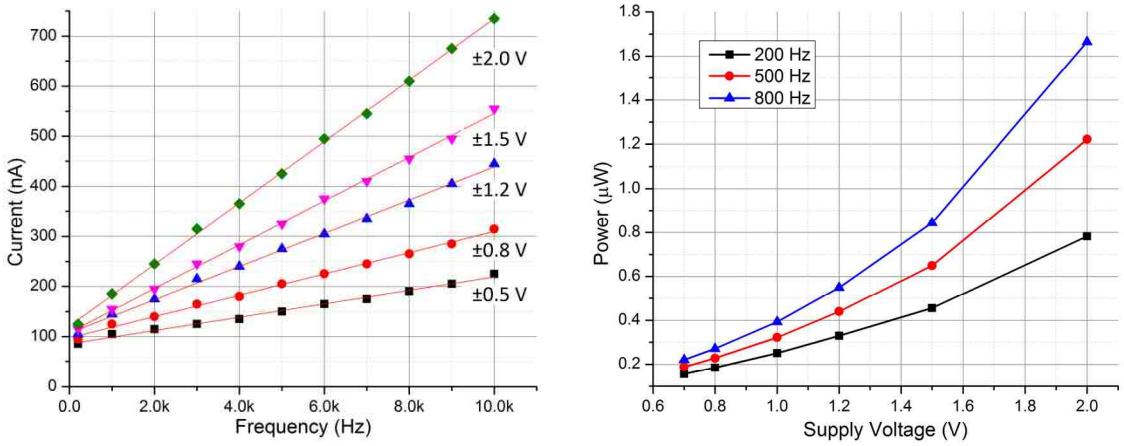
(a)



(b)

Figure 6.14: (a) Layout of the SSHI PCB designed with a DIP40 type IC package footprint for PEHs. (b) Photograph of a populated PCB.

Before characterizing the effect of the SSHI circuit on PEH output, power dissipation of the circuit was measured at different supply voltages and frequencies. Since the circuit consists of only ultra-low power components, accurate current measurement at typical operation frequencies (less than 1 kHz) was difficult. Instead, measurements were done at different frequencies up to 10 kHz, and the results were extrapolated to extract the power dissipation at lower frequencies. Figure 6.15 (a) shows the current drawn by the comparator at different frequencies and supply voltages. Similar measurements were repeated for the pulse generator block and the switch in order to calculate the total power dissipation of the circuit, which is shown in Figure 6.15 (b). It can be seen that using low supply voltages reduce the power dissipation to very low levels; on the other hand, the comparator and the switch require that their inputs do not exceed the supply levels.

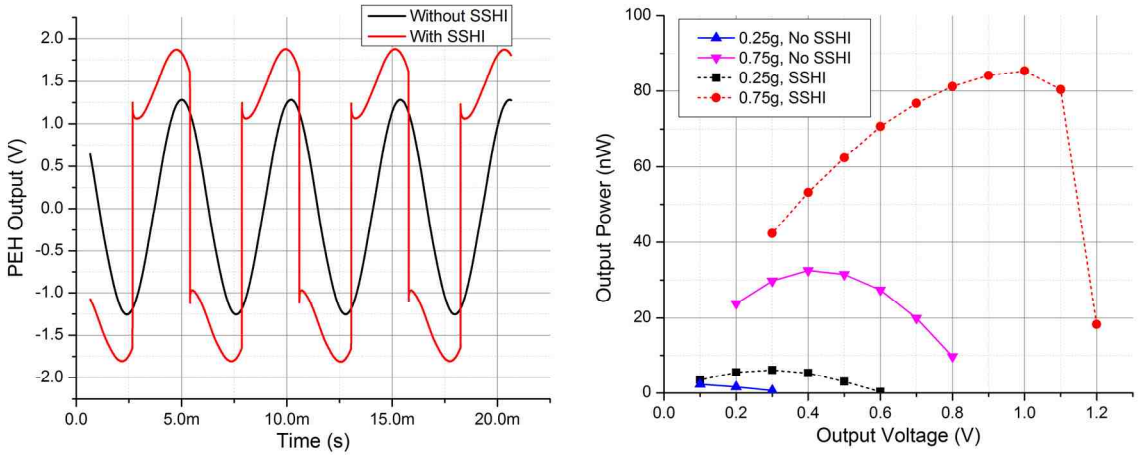


(a) **(b)**

Figure 6.15: (a) Current drawn by the comparator TLV3691 at different frequencies and supply voltages. (b) Total power dissipation of the SSHI circuit with different supply voltages. The circuit consumes only 300 nW power at 200 Hz when operated from ±1.2 V.

The SSHI circuit was tested together with fabricated PEHs in order to verify its proper operation and to evaluate its effect on the power output. Figure 6.16 (a) shows the

output voltage waveform of an 1800 µm × 2000 µm PEH with and without the SSHI when loaded with two standard oscilloscope probes (10 MΩ // 13 pF). It can be seen that the tripping delay is quite small and output voltage is flipped properly, verifying the proper operation of the designed PCB. Figure 6.16 (b) shows the power harvested from the same PEH with and without SSHI. The device was connected to a DC voltage via a full wave rectifier constructed using Schottky diodes in these tests.



(a) **(b)**

Figure 6.16: (a) Output voltage of an 1800 µm × 2000 µm PEH with and without SSHI when loaded with two standard oscilloscope probes. (b) Comparison of the harvested power from the same PEH with and without SSHI. The device was connected to a constant DC voltage through a full wave rectifier constructed using Schottky diodes. Output power was found to be 165% and 162% higher with SSHI at 0.25g and 0.75g input acceleration values.

Maximum harvested power was found as 2.3 nW and 32.5 nW at 0.25g and 0.75g, respectively, when the PEH was connected directly to the rectifier. Maximum harvested power increased to 6.1 nW and 85.3 nW for the same acceleration levels when the SSHI interface was activated, yielding an improvement of approximately 165%. Power dissipation of the SSHI circuit, which was operated from ±1.0 V supplies for these tests, was measured as 250 nW. Although this value is still higher than the maximum harvested

power, it should be noted that the harvested power scales up almost linearly with increasing PEH area whereas the power consumption of the SSHI is independent of the PEH dimensions. To exemplify, a similar PEH with 5 times the area, only 18 mm^2, would yield approximately 425 nW and 165 nW power output with and without the same SSHI circuit, respectively, in response to a 0.25 g input acceleration. On the other hand, power consumption of the circuit would be still approximately 250 nW, slightly smaller than the power gained by SSHI operation. Consequently, the SSHI interface would be providing a net gain in the harvested power for the given example. If the input acceleration or total PEH area were increased further, the power gain would be more significant.

CHAPTER 7: CONCLUSION AND FUTURE WORK

In this work, successful fabrication and operation of CMOS compatible MEMS PEHs were demonstrated using the piezoelectric polymer PVDF-TrFE. The fabrication process was optimized to yield highly uniform and smooth thin films exhibiting strong ferroelectric and piezoelectric properties. A comprehensive characterization study was performed and various dielectric, ferroelectric, and piezoelectric properties of the fabricated films were measured. Two generations of cantilever type d_{31} mode PEHs were designed, fabricated, and tested. Measurement results were compared with theoretical calculations. Different power conditioning circuit topologies were investigated for integration with the fabricated prototypes and parallel SSHI architecture was chosen for this purpose. Two low-power parallel SSHI circuit designs, one at transistor level and the other at board level, were completed. Board level design was implemented on a PCB and its proper operation was verified via experiments conducted using the fabricated PEH prototypes.

In order to develop CMOS compatible MEMS scale PEHs, various design problems were studied. In the early stages of the work, IDE type electrodes were considered in order to utilize the d_{33} mode, which has a higher coupling than d_{31} mode. An FEM based method was developed to examine the effect of IDE pattern on energy harvesting performance [66]. An interesting result was encountered during this study, suggesting that IDE based PEHs were not effectively utilizing the piezoelectric material volume. As a result, later studies were focused on d_{31} mode devices.

Another important decision was the choice of piezoelectric material, which is critical for CMOS compatibility. Four different piezoelectric materials were examined; three of

them, ZnO, AlN, and PVDF-TrFE, are CMOS compatible, whereas the last one, PZT, is not due to its high crystallization temperature. An FEM based comparative study was performed; and the results indicated that ZnO and PVDF-TrFE could outperform AlN for a given layer structure. Considering the other advantages of PVDF-TrFE such as simple fabrication method, low elastic constant, and flexibility, it was chosen for the fabrication of the CMOS compatible MEMS scale PEHs.

Extensive fabrication studies were performed with the selected piezoelectric material in order to optimize the process parameters for high quality films with strong piezoelectric response. Solutions were developed to the problems encountered during the first experiments, including pinholes on the polymer film and weak electrode adhesion. Fabricated high quality films were then characterized in detail. Dielectric constant and dielectric loss were measured at different frequencies. Ferroelectric response was measured with various voltage amplitude and frequencies at different temperatures. Out-of-plane piezoelectric displacement values of the thin films were also measured. Obtained results were compared with previous results reported in the literature and found to be consistent.

After the process optimization of PVDF-TrFE thin films was completed, MEMS scale PEH design studies were started. Substrate was chosen as a 4” Si wafer coated with low stress SiN_x and SiO_2 films. Although theoretical calculations indicated optimal PVDF-TrFE layer thickness values on the order of 7 μm, an upper limit of 1.5 μm was set for the thickness of the polymer considering the limitations in fabrication and poling. Process plan, device design, and mask design for this first generation PEHs were completed accordingly. Despite some problems during fabrication and packaging,

suspended devices were successfully attached to IC packages for the tests, which showed that the ferroelectric and piezoelectric response of the film had not been adversely affected during fabrication. Electromechanical tests were performed by push-and-release type tests conducted using a custom-made probe tip attached to a probe station. Output power density of a (1200 μm × 300 μm) prototype was calculated approximately as 0.1 nW/mm^2 for a sustained tip displacement of 500 μm. Despite the low power output density, test results of the first generation PEHs proved the energy conversion capability of PVDF-TrFE at MEMS scale after going through various microfabrication steps.

The reason for the low power output density of first generation PEHs was known to be the sub-optimal piezoelectric layer thickness. Therefore, design studies were started for a new set of devices with thicker PVDF-TrFE layer and wider surface area. More detailed studies on the layer structure yielded an optimal PVDF-TrFE thickness of approximately 7.4 μm. In order to alleviate the problems that can be brought by such a large step height and to increase unit area capacitance, a multilayer approach was chosen for the second generation devices. In addition, an optimized grayscale lithography recipe was developed for a contact aligner. This recipe was used while patterning the polymer layer in order to create slanted walls on which electrode connections were formed. Slanted walls greatly reduced the problem of electrode discontinuity at PVDF-TrFE edges encountered in the first generation. Fabrication of the second generation multilayer PEHs was completed using similar process steps. Suspended prototypes were connected to standard IC packages and tested using an electrodynamic shaker. Resonance frequencies of the multilayer PEHs were measured between 120 Hz and 950 Hz. Maximum power output density on a purely resistive load at 1.0 g input acceleration was

measured as 27.8 nW/mm^2 from a (1800 μm × 1200 μm) device. Measured voltages were compared with the results of theoretical calculations, and it was concluded that clamping of the piezoelectric material by the substrate improves the power output.

A power conditioning circuit was also designed to improve the harvested energy. Among the different circuit architectures proposed for PEHs, parallel SSHI was chosen because of its simple structure, significant power improvement, and relaxed minimum open circuit voltage requirement. The design of parallel SSHI circuits was done at both transistor level and board level, the former using NCSU CDK design kit in Cadence and the latter in Eagle. The board level design was implemented as PCBs, which were then populated with discrete components and characterized. Power dissipation of the circuit with ±1 V supply voltages was measured as 250 nW when operated at 200 Hz. The same circuit provided an improvement of 165% to the DC power output of a (1800 μm ×1200 μm) prototype. Extrapolated data shows that the circuit becomes feasible for device areas as small as 18 mm^2 for 0.25 g peak input acceleration at resonance frequency.

The power output and reliability of PVDF-TrFE based CMOS compatible MEMS scale PEHs can be improved in a number of ways. First of all, PVDF-TrFE is a highly flexible material that can accommodate high strain levels. A linear stress-strain relationship up to a strain of 15% has been shown for homopolymer PVDF, whereas PZT films typically cannot exceed 0.1% strain [102]. Such high yield strain levels can be also expected for PVDF-TrFE, since its mechanical properties are similar to PVDF. This highly flexible nature of piezoelectric polymers can be exploited to generate higher power outputs [102]. In order to achieve this, novel mechanical structures that can

generate high average strain levels should be investigated. However, it should be noted that the electrodes and other structural layers in the devices must be able to withstand the same strain levels. In addition, mechanical fatigue performance of these materials should be investigated for long term reliability assessment of the devices. For example, a PEH with a resonant excitation average of 6 hours/day at 150 Hz would undergo approximately 6 x 10^9 (6 billion) cycles in 5 years. Such high number of cyclic loading can lead to fatigue damage, especially in devices operating at large strains. To the best of the author's knowledge, there are no studies in literature on the mechanical fatigue performance of PVDF-TrFE thin films. Although low frequency (less than 10 Hz) fatigue data can be found in the datasheets of commercial PVDF films, these data might not be very relevant for PVDF-TrFE based vibration energy harvesters since typical operation frequencies are higher, where thermal effects can be more effective than mechanical effects [134]. On the other hand, more data can be found on the mechanical fatigue performance of more common MEMS materials. Existing studies suggest that low-stress SiN_x thin films do not exhibit degradation up to 10^9 (1 billion) cycles even at stress levels as high as 5 GPa [135]. On the other hand, sputtered Al thin films have been shown to accumulate micro-cracks that result in increased resistance after 10^6 (1 million) cycles [136]. Therefore, while SiN_x seems to be a good candidate for high-strain PEHs, Al electrodes might need to be replaced with more durable alternatives. In this case, process optimization and film characterization studies must be repeated in order to evaluate the piezoelectric performance of PVDF-TrFE with the new electrode material. Although detailed fatigue experiments were not performed in this study, it is worth noting that no

degradation was observed in the power output of prototypes exceeding 10^7 (10 million) resonant excitation cycles.

It was observed that a higher number of devices lost electrode contact during poling in the second generation. This might be because of contact problems around the slanted walls. Normally, all electrodes on a wall should be shorted and therefore, the electric field should be zero between them. If there are floating electrodes in these walls, they might cause large electric fields to develop, causing dielectric breakdown. Therefore, electrode deposition and patterning should be optimized to give better yield.

Fabricated PEH prototypes using the methods and materials described in this study yielded resonance frequencies lower than 200 Hz at dimensions smaller than 2 mm. Therefore, this technology can be adapted to harvest energy at MEMS scale from commonly available ambient vibration sources. Power output density values as high as 30 nW/mm^2 were measured with 1.0 g harmonic acceleration amplitudes. Suggested future studies can result in improvements in the power output density and reliability of PVDF-TrFE based MEMS scale PEHs. Such improvements, along with the CMOS compatibility of the polymer, can allow the fabrication of monolithically integrated devices for sustainable electronics. This approach can be used to alleviate or even eliminate the limitations of the batteries and lead to the development of self-sustained electronics, which can find use in various applications such as WSNs, wide area surveillance systems, or consumer electronics.

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