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Performance improvement of single-phase PLLs under adverse grid conditions: An FIR filtering-based approach

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ABSTRACT

With ever-increasing power quality problems in power systems, which are mainly attributable to the proliferation of nonlinear power electronics-based loads and also the high penetration of renewable energy sources in the utility grid, more advanced phase-locked loops (PLLs) for the synchronization of power converters and/or extraction of fundamental parameters of the grid voltage are needed. To this end, using a finite-impulse-response filter, which includes an arbitrary number of filter modules, is proposed in this paper. The design procedure for the proposed filter is explained in detail, and its effectiveness is investigated by applying it to a well-known single-phase PLL, the enhanced PLL (EPLL), and performing some comparative simulation and experimental tests. The obtained results demonstrate that the proposed filter can significantly enhance the filtering capability of the EPLL while preserving a fast dynamic behavior.

1. Introduction

It is not an exaggeration to state that the phase-locked loop (PLL) is the first choice for the synchronization of power converters to the grid. This popularity is mainly because of the ease of digital implementation of PLLs and also the simplicity of their stability analysis and tuning procedure [1]. Focusing on single-phase applications, the PLLs can be classified into three major categories: 1) power-based PLLs (pPLLs); 2) and quadrature signal generation-based PLLs (QSG-PLLs). A brief review of these categories is presented below.

The key characteristic of pPLL is having a product-type phase detector (PD) [2]. This PD, nevertheless, causes a large double-frequency component in the pPLL control loop, which results in double-frequency oscillatory ripples in the pPLL estimated quantities. To tackle this issue, some advanced pPLLs have been designed and proposed recently. Indeed, the main difference of these PLLs lies in the technique they use for rejecting the aforementioned double-frequency component. Including a moving average filter (MAF) into the pPLL control loop and using a variable sampling frequency [3,4], incorporating the *dq*-frame delayed signal cancellation operator into the pPLL control loop [5], and employing a *dq*-frame adaptive low-pass/notch filter, known as the double-frequency and amplitude compensation (DFAC) method, in the pPLL structure [6] are some examples of such techniques.

The QSG-PLLs are probably the most widely used single-phase PLLs in power and energy applications. The basic idea behind these PLLs is creating a fictitious quadrature signal for transferring information into the *dq*-frame. The main difference between these PLLs lies in the technique they use for creating the quadrature signal. Using the Kalman filter, transfer delay, low-pass filter, all-pass filter, and Hilbert transform are some available quadrature signal generators [7,8]. Another member of QSG-PLLs, which has a different structure than others, is the enhanced PLL (EPLL). This PLL has been developed based on an optimization perspective [9,10]. The EPLL, in addition to the grid voltage phase and frequency, provides an estimation of the grid voltage amplitude which enables that to completely remove the double-frequency oscillatory error. Advanced versions of the EPLL can be found in [11,12].

In recent years, with ever increasing power quality issues in power systems, which are mainly because of the proliferation of nonlinear power electronics-based loads and also the high penetration of renewable energy sources in the utility grid, more advanced PLLs for the control and synchronization purposes are required. To deal with this challenge, some research efforts have been made by different research groups. For instance, inspired by the work in [13], a fast response single-phase PLL with the ability to reject the dc component is proposed in [14]. The key idea in [14] is using two wide-bandwidth second-order generalized integrator (SOGI) based bandpass filter before the PLL input to block the dc offset without slowing down the dynamic response

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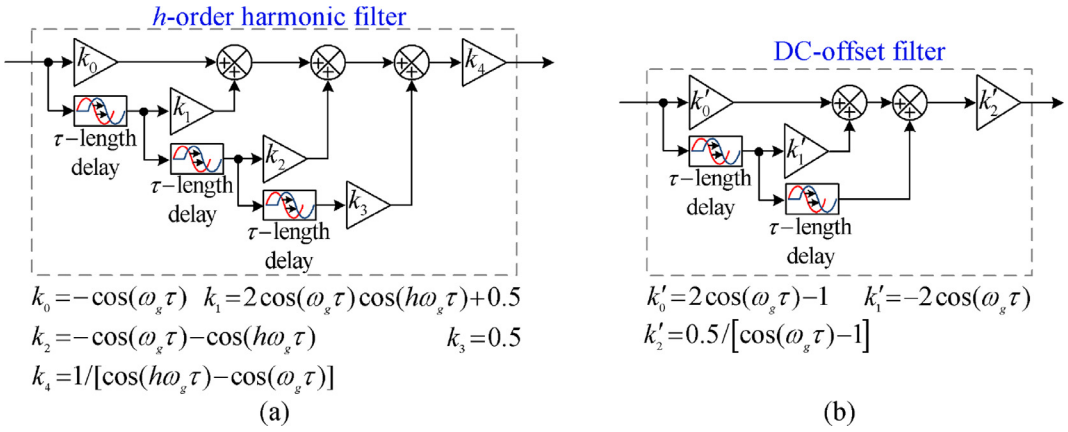

Fig. 1. Time-domain implementation of the proposed FIR filter for rejecting (a) the *h*-order harmonic component and (b) the dc offset.

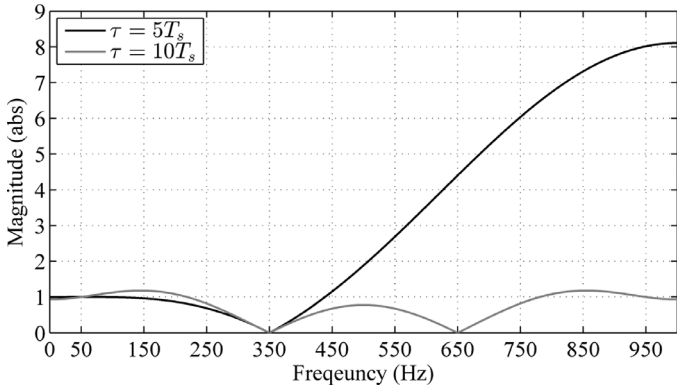

Fig. 2. Magnitude-frequency response of $F_7(s)$ for two different values of τ. T_s is the sampling period and it is considered to be 0.1 ms.

too much. The problem is that these SOGIs are nonadaptive. Therefore, this approach may be useful only in applications where the grid frequency changes are very limited. In [15], a modified PLL based on a combination of the non-frequency-dependent transfer delay (NTD) concept, moving average filter, and phase lead compensator is proposed. Using these elements, which all require storing a large number of samples in the memory, implies that the proposed PLL in [15] requires a high memory requirement, even when the sampling frequency is not very high. Some more works in this area can be found in [16] and [17].

In this paper, a finite impulse response (FIR) filter to improve the performance of single-phase PLLs under adverse grid conditions is presented. To verify the effectiveness of the proposed filter, it is applied to the EPLL and the obtained results are compared with those of an advanced EPLL [11].

2. Proposed filtering strategy

2.1. Harmonic filtering

To simplify the design procedure, the single-phase voltage signal is considered to be as

$$v(t) = \underbrace{V_1\cos(\theta_1)}_{v_1(t)} + \underbrace{V_h\cos(\theta_h)}_{v_h(t)} \tag{1}$$

where $v_1(t)$ [$v_h(t)$] denotes the fundamental component [*h*th harmonic component] in the single-phase voltage signal, and θ_1 and V_1 [θ_h and V_h] are the phase angle and amplitude of the fundamental component [*h*th harmonic component], respectively. Here, for the sake of simplicity, θ_1 and θ_h are defined as $\theta_1 = \omega_g t + \varphi_1$ and $\theta_h = h\omega_g t + \varphi_h$, where ω_g is the fundamental angular frequency and φ_1 and φ_h are initial phase angles.

Delaying the single-phase signal (1) with time delay τ, 2τ, and 3τ results in

$$\begin{aligned} v(t-\tau) = {} & \cos(\omega_g\tau)v_1(t) + \sin(\omega_g\tau)qv_1(t) \\ & + \cos(h\omega_g\tau)v_h(t) + \sin(h\omega_g\tau)qv_h(t) \end{aligned} \tag{2}$$

$$\begin{aligned} v(t-2\tau) = {} & \cos(2\omega_g\tau)v_1(t) + \sin(2\omega_g\tau)qv_1(t) \\ & + \cos(2h\omega_g\tau)v_h(t) + \sin(2h\omega_g\tau)qv_h(t) \end{aligned} \tag{3}$$

$$\begin{aligned} v(t-3\tau) = {} & \cos(3\omega_g\tau)v_1(t) + \sin(3\omega_g\tau)qv_1(t) \\ & + \cos(3h\omega_g\tau)v_h(t) + \sin(3h\omega_g\tau)qv_h(t) \end{aligned} \tag{4}$$

where $v_1(t) = V_1\cos(\theta_1)$, $qv_1(t) = V_1\sin(\theta_1)$, $v_h(t) = V_h\cos(\theta_h)$, and $qv_h(t) = V_h\sin(\theta_h)$.

Equations (1) -(4) can be rewritten in the matrix form as (5).

$$\begin{bmatrix} v(t) \\ v(t-\tau) \\ v(t-2\tau) \\ v(t-3\tau) \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 & 1 & 0 \\ \cos(\omega_g\tau) & \sin(\omega_g\tau) & \cos(h\omega_g\tau) & \sin(h\omega_g\tau) \\ \cos(2\omega_g\tau) & \sin(2\omega_g\tau) & \cos(2h\omega_g\tau) & \sin(2h\omega_g\tau) \\ \cos(3\omega_g\tau) & \sin(3\omega_g\tau) & \cos(3h\omega_g\tau) & \sin(3h\omega_g\tau) \end{bmatrix}}_{\boldsymbol{W}} \begin{bmatrix} v_1(t) \\ qv_1(t) \\ v_h(t) \\ qv_h(t) \end{bmatrix}. \tag{5}$$

By multiplying both sides of (5) by the inverse of $\boldsymbol{W}$, the

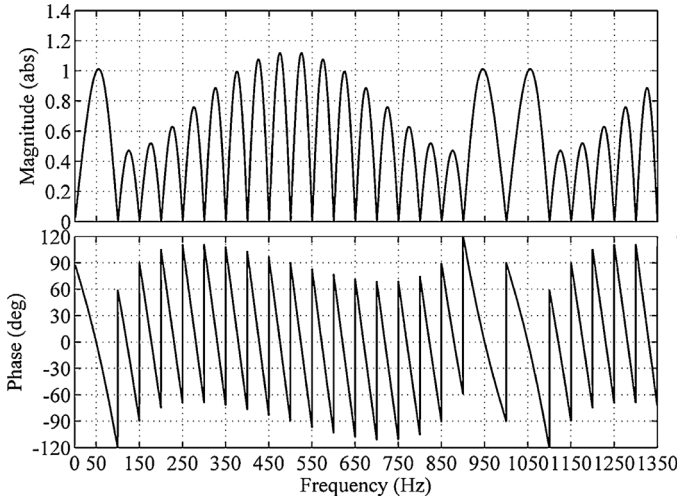

Fig. 3. Frequency response of the chain of selected filter modules.

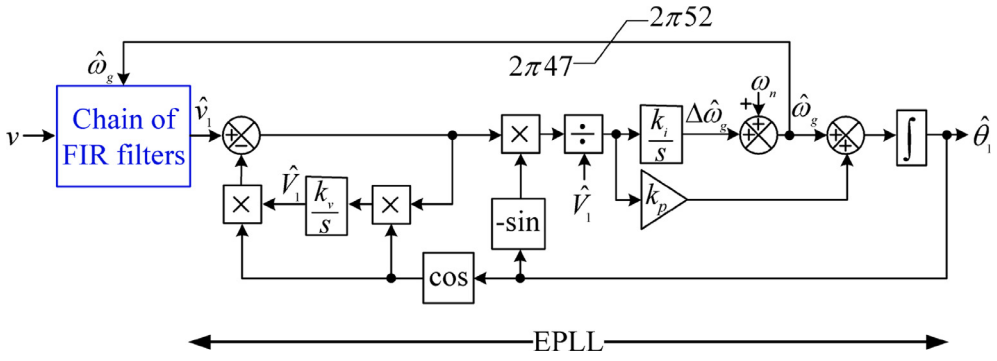

Fig. 4. Schematic diagram of the EPLL with the chain of designed FIR filters, which is briefly referred to as the FIR-EPLL.

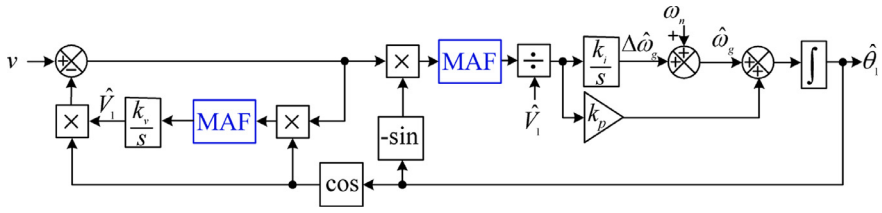

Fig. 5. Schematic diagram of the MAF-EPLL.

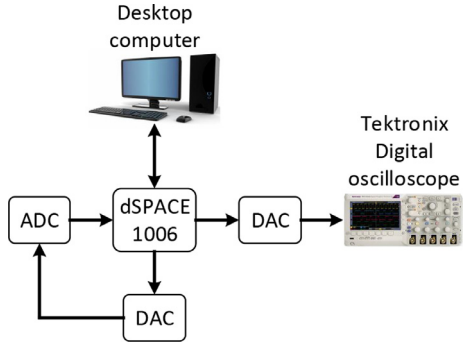

Fig. 6. Experimental setup..

fundamental component $v_1(t)$, the harmonic component $v_h(t)$, and their quadrature versions can be expressed based on the single-phase signal $v(t)$ and its delay versions. Here, we are only interested in extracting the fundamental component, which can be expressed as

$$v_1(t) = k_4[k_0 v(t) + k_1 v(t-\tau) + k_2 v(t-2\tau) + k_3 v(t-3\tau)] \quad (6)$$

Table 1
Control Parameters.

	FIR-EPLL	MAF-EPLL
Integral gain, k_i	71061	5687
Proportional gain, k_p	1055	165.7
Gain of voltage estimation loop, k_v	1055	165.7
Window length of MAFs, T_w	—	10 ms
Delay length of harmonics/dc-offset filters, τ	1 ms / 5 ms	—

where $k_0 = -\cos(\omega_g\tau)$, $k_1 = 2\cos(\omega_g\tau)\cos(h\omega_g\tau) + 0.5$, $k_2 = -\cos(\omega_g\tau) - \cos(h\omega_g\tau)$, $k_3 = 0.5$, and $k_4 = 1/[\cos(h\omega_g\tau) - \cos(\omega_g\tau)]$. The time-domain implementation (6), which describes the proposed FIR filter for rejecting a harmonic component of order h, can be observed in Fig. 1(a).

In designing the proposed filter, only a single harmonic in the grid voltage was considered. In practice, however, there are often several harmonic components in the grid voltage. To deal with this situation, several modules of the proposed filter [Fig. 1(a)] can be cascaded to each other.

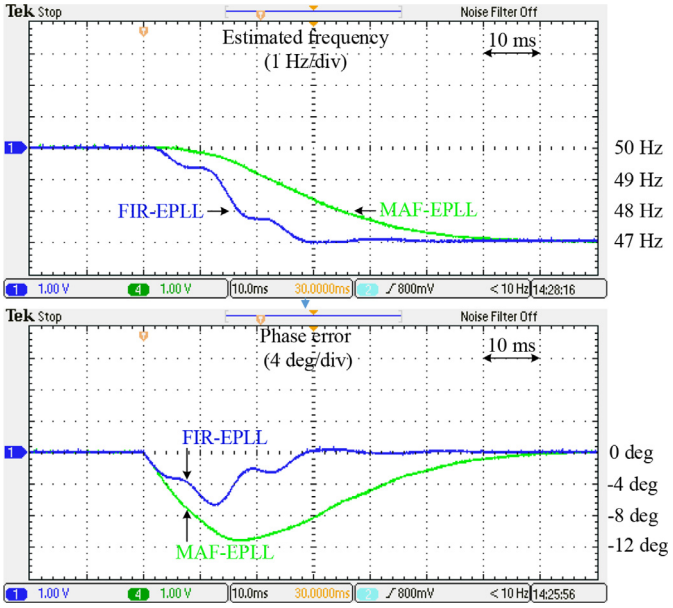

Fig. 7. Experimental results in response to test case 1.

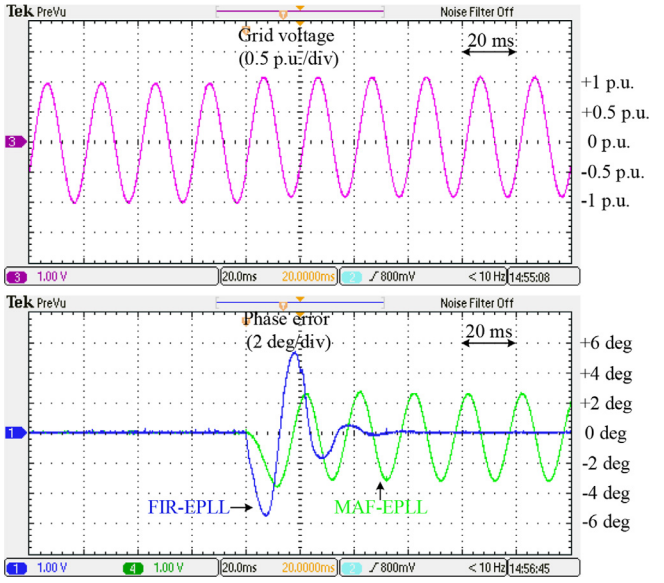

Fig. 8. Experimental results in response to test case 2.

2.2. DC-Offset Filtering

Assume that the single-phase signal is as

$$v(t) = V_1 \cos(\theta_1) + v_{dc} \tag{7}$$

where v_{dc} denotes the dc component, which is assumed to be a constant.

Delaying the single-phase signal (7) with time delay τ and 2τ and arranging the results in the matrix form gives

$$\begin{bmatrix} v(t) \\ v(t-\tau) \\ v(t-2\tau) \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 & 1 \\ \cos(\omega_g\tau) & \sin(\omega_g\tau) & 1 \\ \cos(2\omega_g\tau) & \sin(2\omega_g\tau) & 1 \end{bmatrix}}_{G} \begin{bmatrix} v_1(t) \\ qv_1(t) \\ v_{dc} \end{bmatrix}. \tag{8}$$

Multiplying both sides of (8) by the inverse of $\boldsymbol{G}$ gives the proposed filter for rejecting the dc-offset as

$$v_1(t) = k_2'[k_0'v(t) + k_1'v(t-\tau) + v(t-2\tau)] \tag{9}$$

where $k_0' = 2\cos(\omega_g\tau) - 1$, $k_1' = -2\cos(\omega_g\tau)$, and $k_2' = 0.5/[\cos(\omega_g\tau) - 1]$. The time-domain implementation of the proposed FIR filter for rejecting the dc component can be observed in Fig. 1(b).

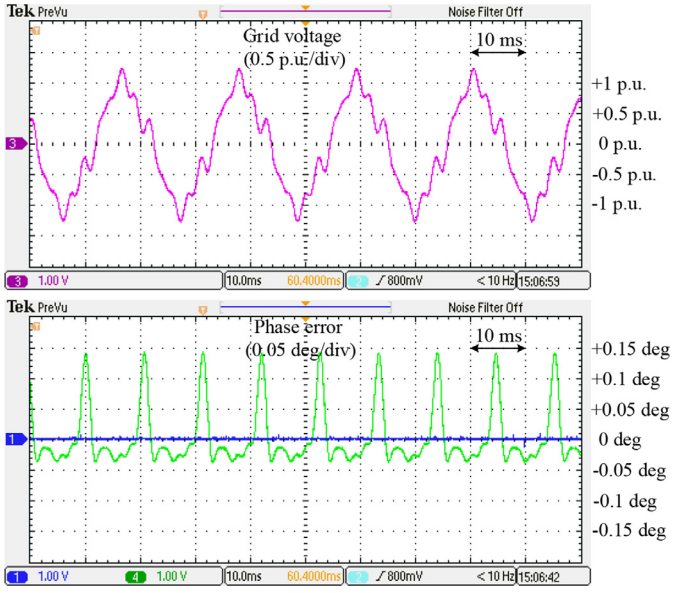

Fig. 9. Experimental results in response to test case 3.

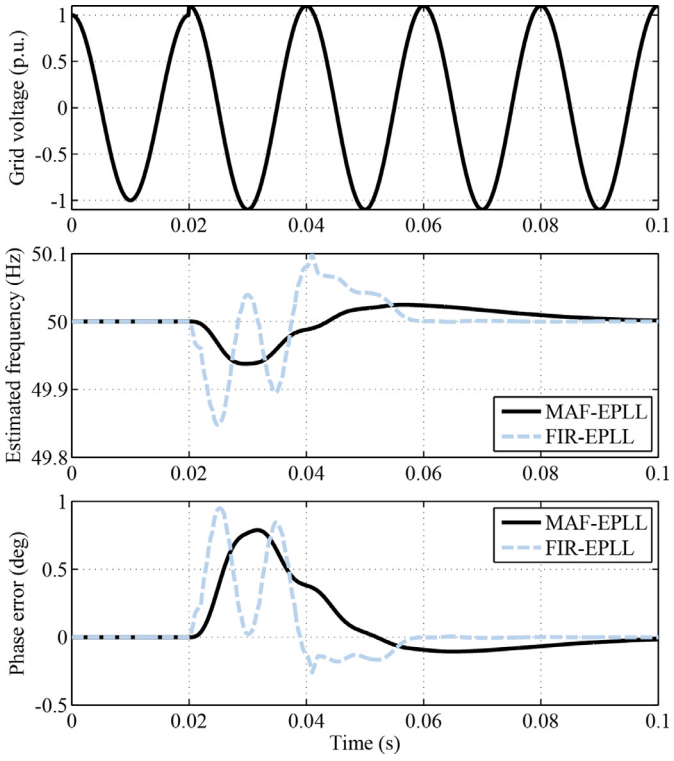

Fig. 10. Simulation results in response to 0.1 p.u voltage swell.

2.3. Guidelines

An issue that should be discussed here is choosing the number of filter modules and their delay length. Selecting the number of filter modules involves a tradeoff between the filtering capability and computational burden: the harmonic filtering capability can be improved by increasing the number of filter modules but at the cost of an increased computational effort. Regarding the delay length τ, the selection mainly involves a tradeoff between the noise immunity and the speed of

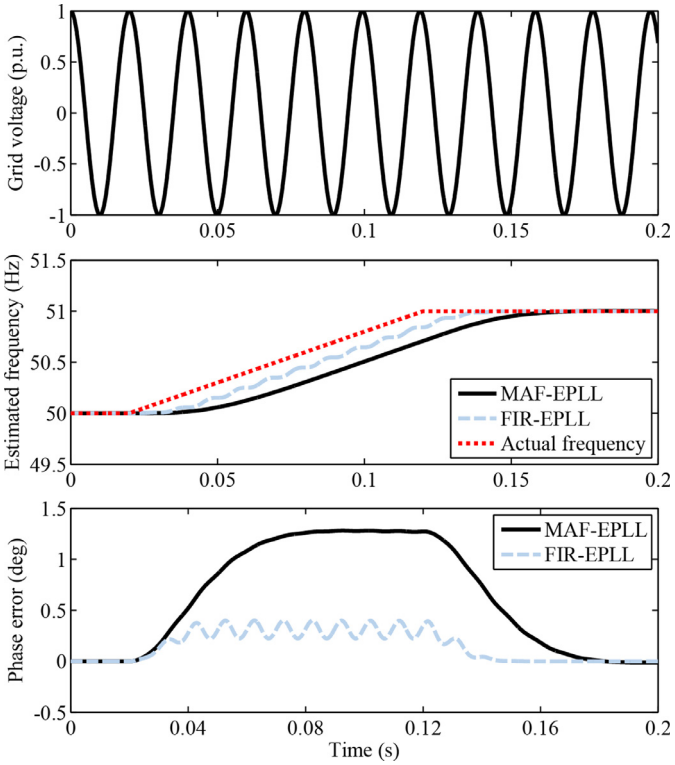

Fig. 11. Simulation results in response to a frequency ramp of 10 Hz/s for 0.1 s.

Table 2
Details of Experimental and Simulation Regards .

	FIR-EPLL	MAF-EPLL
Frequency jump test		
2% settling time	28 ms	61 ms
Phase overshoot	6.75°	11.3°
Dc offset test		
Peak-to-peak steady-state frequency error	0 Hz	0.56 Hz
Peak-to-peak steady-state phase error	0°	5.9°
Harmonic distortion test		
Peak-to-peak steady-state frequency error	0 Hz	0.02 Hz
Peak-to-peak steady-state phase error	0°	0.2°
Voltage swell test		
Response time	≈ 2 cycles	≈ 4 cycles
Frequency ramp test		
Frequency error during frequency ramp	≈ 0.15 Hz	≈ 0.3 Hz
Phase error during frequency ramp	≈ 0.3°	≈ 1.3°

response: increasing the delay length τ improves the noise immunity of the cascaded filter modules but at the cost of slowing down the dynamic response. Another factor that should be considered in choosing the delay length τ is the extra harmonics that each filter, in addition to its main responsibility, can reject. To better visualize this fact, Fig. 2 shows the magnitude-frequency response of the proposed filter for rejecting the seventh-order harmonic for two different values of τ. As shown, regardless of the value of τ, the proposed filter passes the fundamental (50 Hz) component and rejects the seventh-order harmonic (350 Hz) component. Nevertheless, it can be observed that selecting a higher value for τ results in rejecting additional harmonic(s).

Altogether, selecting the number of filter modules and their delay length is an optimization problem in which factors such as computational burden, noise immunity, dynamic response, and filtering capability should be considered. Here, five filter modules for rejecting the dc component and third, fifth, seventh, and ninth-order harmonics are recommended. The delay length τ in all harmonic filters is chosen to be $\tau = T/20$ (T is the grid fundamental period). In the case of dc filter, nevertheless, the delay length is chosen to be $T/4$. The frequency response of this chain of filter modules can be observed in Fig. 3. As shown, these filters in addition to their main tasks (i.e., removing the dc offset and third, fifth, seventh, and ninth-order harmonics) block almost all other harmonics in the grid voltage. It should be mentioned that the odd-order harmonics of order 19, 21, 39, 41, ⋯ are not blocked by the chain of filters. It is not a serious issue because these harmonics have a small magnitude in most practical cases.

3. Simulation and experimental results

To evaluate the effectiveness of the proposed filtering strategy, it is applied to the enhanced PLL (EPLL), as shown in Fig. 4, and some experimental and simulation tests are conducted. A sampling frequency of 10 kHz is considered for obtaining the simulation and experimental results. As a reference for comparison, an advanced EPLL, which is here called the MAF-EPLL, is considered [11]. The schematic diagram of the MAF-EPLL can be observed in Fig. 5. Notice that the MAF is a rectangular window filter with the s-domain transfer function $G_{MAF}(s) = \frac{1-e^{-T_w s}}{T_w s}$. The MAF passes the dc component of its input and completely blocks all frequency components that their frequency is an integer multiple of the inverse of its window length. This feature has made it very popular in designing advanced synchronization systems.

The experimental tests are conducted using dSPACE 1006 platform. The dSPACE, as shown in Fig. 6, is linked with a PC, and is programmed using Matlab/Simulink. Controlling the dSPACE is carried out from its control desk. To have a high flexibility in generating different disturbances for testing the PLLs under study, the single-phase grid voltage signal is generated digitally inside the dSPACE. To take into account the analog-to-digital conversion noise, this signal is converted to an analog one using the DAC board, and sensed as the input of PLLs under study using the ADC unit. The algorithms of PLLs, which have been converted to the C/C++ language files by dSPACE TargetLink tool, are processed by the dSPACE. The output signals, which need to be shown, are sent out using the DAC port of dSPACE and are displayed on a digital oscilloscope [Tektronix DPO 2014B].

The control parameters of both EPLLs are summarized in Table 1.

Three experimental test cases are considered:

- Test case 1: A frequency step change of − 3 Hz happens in the grid voltage.
- Test case 2: 0.1 p.u. dc component is suddenly added to the grid voltage.
- Test case 3: The grid voltage is contaminated with odd-order harmonics of order 3, 5, 7, and 9. The magnitude of all harmonics is 0.1 p.u. The grid frequency is fixed at 47 Hz during this test.

Table 3
A qualitative comparison between the FIR-EPLL, MAF-EPLL, SOGI-FLL-WPF, and robust NTD-PLL.

	Dynamic Response	DC rejection	Harmonic filtering	Interharmonic filtering	Computational burden	Memory Requirement
FIR-EPLL	Fast	Perfect	Perfect	Weak	Average	Depends on the sampling frequency
MAF-EPLL	Slow	Weak	Good	Average	Average	Depends on the sampling frequency
SOGI-FLL-WPF [13]	Average	Perfect	Good	Average	Low	Low
Robust NTD-PLL [15]	Fast	Perfect	Perfect	Weak	Average	Depends on the sampling frequency

Fig. 7 shows the obtained results for test case 1. As can be seen, the FIR-EPLL provides a much faster dynamic response. Fig. 8 compares the performance of PLLs under test case 2. It can be observed that the FIR-EPLL benefits from an excellent dc offset rejection capability. The MAF-EPLL, however, suffers from a large fundamental-frequency oscillatory error in its estimated quantities, which implies it has a limited dc offset rejection capability. This problem, of course, can be alleviated by selecting a window length equal to the grid fundamental period for the MAFs in the MAF-EPLL. This measure, however, makes the dynamic response of the MAF-EPLL extremely slow. The obtained results for test case 3 can be seen in Fig. 9. Both PLLs, particularly the FIR-EPLL, represent a good harmonic filtering capability.

To further investigate the effectiveness of the proposed chain of FIR filters, some more tests are performed in Matlab/Simulink. In Fig. 10, the simulation results of the FIR-EPLL and MAF-EPLL in response to 10% voltage swell are observed. As shown, the FIR-EPLL reaches the steady state faster than the MAF-EPLL. The transient behavior of the MAF-EPLL, however, is more smooth. In Fig. 11, a comparison between the FIR-EPLL and MAF-EPLL in response to a 10 Hz/s frequency ramp is performed. It is observed that the FIR-EPLL can follow the grid frequency with a lower error during the frequency ramp, and has a lower phase error during the frequency ramping interval.

The proposed chain of the FIR filter, as it was shown, can considerably enhance the performance of single-phase PLLs. It, however, has a limitation, which needs to be briefly discussed here. As can be observed in Fig. 1, the implementation of the proposed filter involves using some delays. These delays in practice are implemented by storing $N = \tau/T_s$ samples in the DSP memory, where τ is the delay length, and T_s is the sampling time. It means that by increasing the sampling frequency (which is corresponding to reducing the sampling time), the number of stored samples N increases. It implies that the proposed chain of FIR filter may require a high memory requirement in high sampling frequencies. It is the main limitation of the proposed filter.

Table 2, which summarizes the details of the experimental and simulations results, and Table 3, which provides a qualitative comparison between the FIR-EPLL, MAF-EPLL, SOGI-based frequency-locked loop with prefilter (SOGI-FLL-WPF) [13], and the robust non-frequency-dependent transfer delay PLL (NTD-PLL) [15], provide a deeper insight into the properties of the proposed technique compared to the state-of-the-art solutions.

4. Conclusion

In this paper, an FIR filtering technique for improving the disturbance rejection capability of single-phase PLLs was proposed. The study was started with discussing the design procedure for the proposed filter. For the sake of clarity, the design procedure was divided into two distinct stages: 1) the h-order harmonic filter design, and 2) the dc-offset filter design. Some guidelines for selecting the number of filter modules and their delay length were then presented. Finally, to demonstrate the effectiveness of the proposed filter, it was applied to the EPLL, which is a well-known single-phase PLL. The resulting PLL was named the FIR-EPLL, and its results were compared to the MAF-EPLL under some typical tests. It was demonstrated that the FIR-EPLL offers a better performance than the MAF-EPLL in terms of both dynamic response and filtering capability. These observations confirm the effectiveness of the proposed filter.

CRediT authorship contribution statement

Hamed Sepahvand: Conceptualization, Methodology, Software, Validation, Writing - original draft. **Mohsen Saniei:** Writing - review & editing, Conceptualization, Supervision. **Seyed Saeidollah Mortazavi:** Writing - review & editing, Conceptualization, Supervision. **Saeed Golestan:** Writing - review & editing, Software, Validation.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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